MOSTEK
CORPORATION

MOS Integrated Circuits

1215 W. Crosby Road, Carrollton, Texas 75006

MOSTEK ®

MOS INTEGRATED CIRCUITS

PRODUCT GUIDE

MOSTEK CORPORATION

OCTOBER/1972

STANDARD PRODUCT LINE

		ION IMPLANTED	DEPLETION LOAD
Shift Registers			
MK 1002 P, L	2x128-Bit Static	✓	
MK 1007 P	4x80-Bit Dynamic	✓	
***Read-Only Memories**			
MK 2002 P	Column-Out Character Generator		
MK 2302 P	Column-Out Character Generator	✓	
MK 2400 P	2560-Bit ROM	✓	
MK 2408 P	Row-Out Character Generator	✓	
MK 2500 P	4096-Bit ROM	✓	✓
MK 2600 P	4096-Bit ROM	✓	✓
Random-Access Memories			
MK 4002 P	64x4 Static RAM	✓	
MK 4006 P	1024x1 Dynamic RAM	✓	✓
MK 4007 P	256x1 Static RAM	✓	✓
MK 4008 P	1024x1 Dynamic RAM	✓	✓
Timing/Display Circuits			
MK 5002/5/7 P	4-Digit Counter Latch Decoder	✓	✓
MK 5009 P	Counter Time Base	✓	✓
MK 5017 P	Programmable Digital Clock	✓	✓
Calculator Circuits			
MK 5010 P	10-Digit, Four Function	✓	
MK 5012 P	12-Digit, Four Function	✓	
MK 5013 P, MK 5014 P	12-Digit, Four Function With Memory	✓	
MK 5015 P	Printing Calculator Interface	✓	
Soon to be Announced			
MK 4012 P	32x8 FIFO Buffer Memory	✓	✓
MK 5020/21 P	8 or 10-Digit, Low Power, 4-Function Calculator	✓	✓

*All ROMs are mask-programmable for custom-encoding to meet customer requirements.

NOTE: Product number suffixes indicate packaging. Numbers ending in "P" are ceramic dual-in-line; "L" are TO-100; "F" are flat-pack.

MOSTEK ION IMPLANTATION

Ion implantation is a processing step by which standard P-channel diffused MOS devices are made directly compatible with TTL/DTL logic. A highly controllable process, it allows the adjusting of gate threshold voltages and also allows the fabrication of both enhancement-mode and depletion-mode transistors on the same chip.

In the Mostek process, silicon wafers are doped with ions of phosphorus or boron, accelerated to high energy levels of 40,000 to 300,000 electron-volts. Penetration depth of the ions is determined by their energy. Areas where implantation is not desired are masked with aluminum or thick silicon oxide.

By implanting ions in the channel region of a transistor (thin oxide area), Mostek reduces the threshold voltage of that transistor without affecting any other device characteristics. Control of atom count enables a high degree of accuracy in the process, allowing the threshold voltage to be set at the desired level. TTL/DTL-compatible devices are so designed that 5-Volt logic swings will turn the transistors on and off and still maintain good noise margins.

CUSTOM-DESIGNED MOS/LSI

Its ion-implantation capabilities and its talented team of MOS design engineers have enabled MOSTEK to become an established leader in custom MOS/LSI, developing many state-of-the-art circuits to satisfy unique customer requirements. MOSTEK offers its customers assistance in optimizing and partitioning existing or proposed logic systems for effective MOS/LSI implementation. Emphasis is placed during design and layout on achieving reproducible parts for high-volume manufacture.

CUSTOM-PROGRAMMED ROM's

All Mostek Read-Only Memories can be custom-programmed to individual customer specifications by coding a single mask used during processing. Coding sheets are available from Mostek offices or representatives (see Page 4).

ABOUT MOSTEK

Mostek was organized to provide LSI users with superior MOS/LSI circuits designed for improved performance and reliability which, in turn, enable the user to offer a superior product. To do this, Mostek has assembled an exceptionally competent engineering staff with deep roots in both IC design and semiconductor processing. This team takes pride in its creative and innovative solutions to customer problems, and has made several highly significant contributions to MOS technology. Among the "firsts" achieved by Mostek are:

- ☐ *The first volume production utilizing ion-implant process*
- ☐ *The first TTL-compatible 1024-bit Random Access Memory*
- ☐ *The first single-chip LSI calculator*
- ☐ *The first MOS/LSI to operate from a single +5V power supply*
- ☐ *The first two-chip calculator with memory*
- ☐ *The first programmable digital clock circuit*

Represented by

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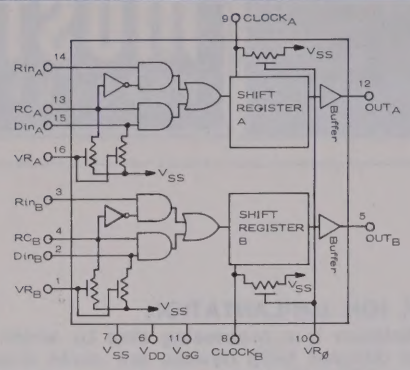
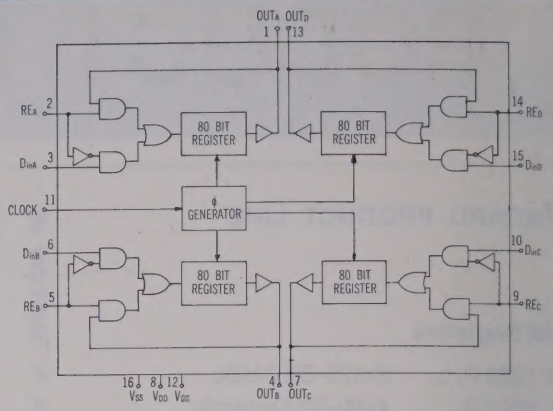
MOSTEK CORPORATION ®

SHIFT REGISTERS



MK 1002 P / STATIC SHIFT REGISTER

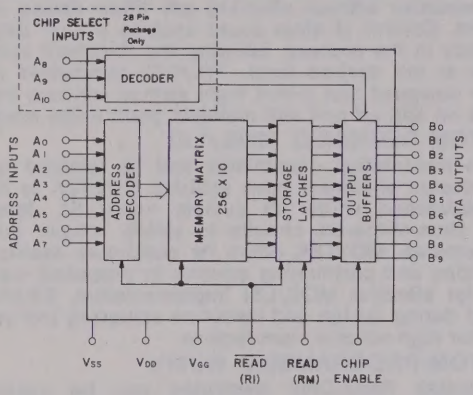
- Dual 128-bit registers
- Ion-implanted for TTL/DTL compatibility
- DC to 1 MHz Clock Rates
- Single-phase TTL-level clock
- Power supply: +5V; −12V
- Package: 16-pin CDIP
- MK 1002 L available, less recirculate logic, in 10-pin TO-100 package



MK 1007 P / DYNAMIC SHIFT REGISTER

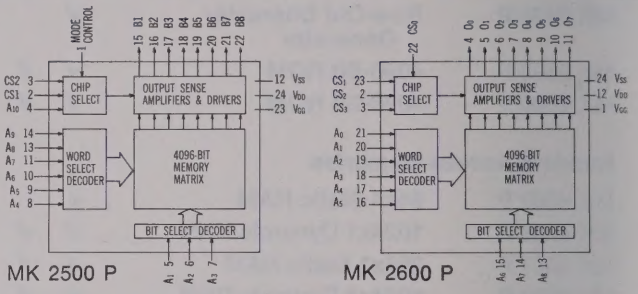
- Quad 80-bit registers
- Ion-implanted for full TTL/DTL compatibility
- Clock rate to 2.5 MHz
- Single-phase TTL-level clock
- Recirculate built-in
- Power supply: +5V, −12V
- Package: 16-pin CDIP

READ-ONLY MEMORIES



MK 2400 P SERIES / 2560-BIT READ-ONLY MEMORIES

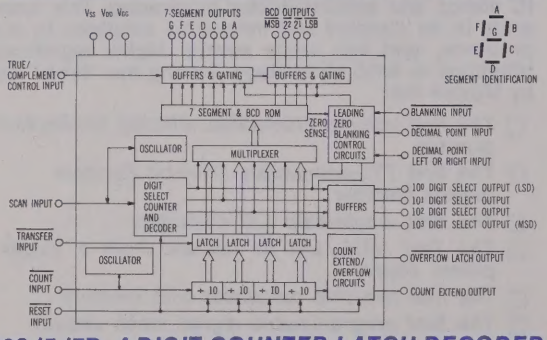
- 256x10 organization
- Ion-implanted for full TTL/DTL compatibility
- 550 ns cycle time, 600 ns access time
- Custom encoding available
- Power supply: +5V, −12V
- Package: 24-pin or 28-pin CDIP



MK 2500 P SERIES / MK 2600 P SERIES / 4906-BIT READ-ONLY MEMORIES

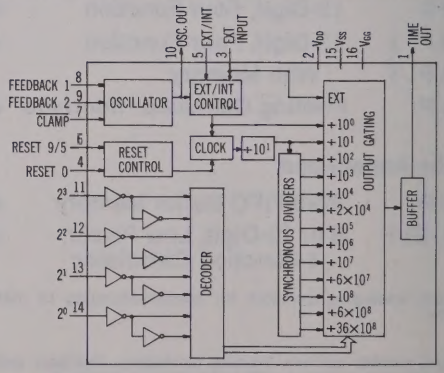
- MK 2500 P Series is pin/pin replacement for National MM 5232
- MK 2600 P Series is pin/pin replacement for Fairchild 3514
- 512x8 organization
- 1024x4 organization optional with 2500 Series
- 500 ns access time, typical
- Ion-implanted depletion loads for low power
- Package: 24-pin CDIP
- Custom encoding available
- Power supply: +5V, −12V

TIMING/DISPLAY CIRCUITS



MK 5002/5/7P 4-DIGIT COUNTER LATCH DECODER

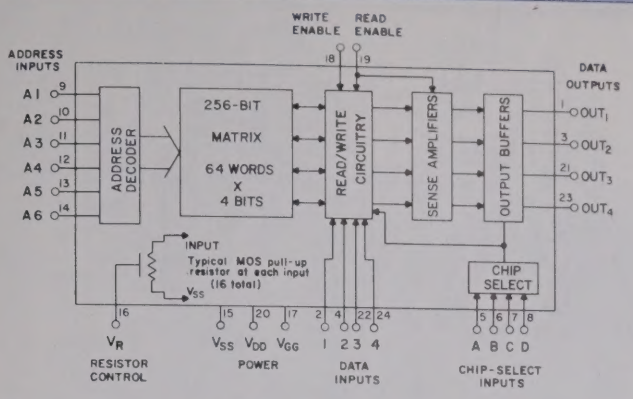
- Ion-implanted for: TTL/DTL compatibility, Single +5V operation, Low power (25 mW)
- On-chip oscillators for scan control and for counter input time base
- MK 5002 P provides 7-segment and BCD outputs in a 28-pin CDIP package
- MK 5005 P provides 7-segment outputs in a 24-pin CDIP package
- MK 5007 P provides BCD outputs in a 16-pin CDIP package. Blanking, Decimal, and Complement controls excluded.



MK 5009 P / COUNTER TIME-BASE CIRCUIT

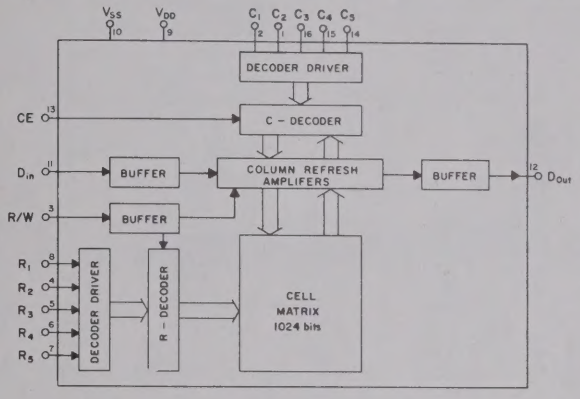
- Ion-implanted for full TTL/DTL compatibility
- Internal clock operates from: External signal, External RC network, External crystal
- Operates DC to above 1 MHz
- Binary-encoded for frequency selection
- Power supply: +5V, −12V
- Package: 16-pin CDIP

RANDOM ACCESS MEMORIES



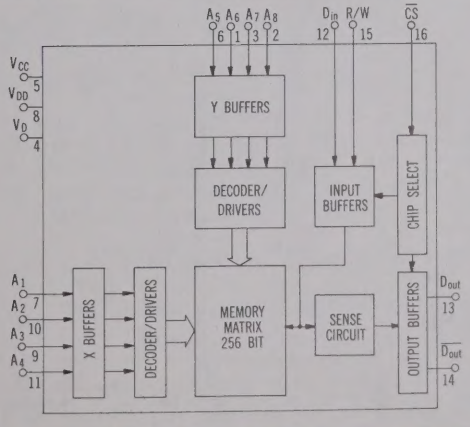
MK 4002 P / 256 (64x4) STATIC RANDOM ACCESS MEMORY

- Ion-implanted for full TTL/DTL compatibility
- Under 1 μsec access and cycle times
- Internal address decoder
- Power supply: +5V, −12V



MK 4006 / MK 4008 P
1024x1 DYNAMIC RANDOM ACCESS MEMORY

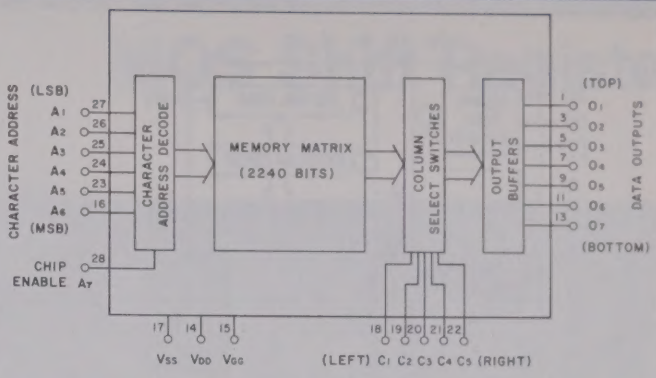
- Ion-implanted for TTL/DTL compatibility
- Access time: MK 4006 P, 400 ns; MK 4008 P, 500 ns
- No clocks required
- Internal address decoders
- Power supply: +5V, −12V
- Package: 16-pin CDIP



MK 4007 P / 256x1 STATIC RANDOM ACCESS MEMORY

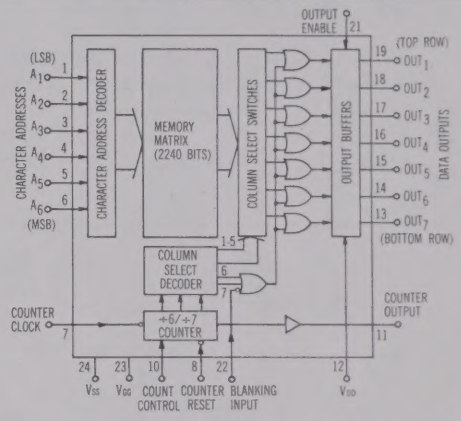
- Ion-implanted for full TTL/DTL compatibility
- Replaces 1101 types pin/pin
- Lower power: 250 mW max. at +5V and −9V
- Higher speed: typical access 450 ns
- Power supply: +5V; −7 to −15V

ROM/CHARACTER GENERATORS



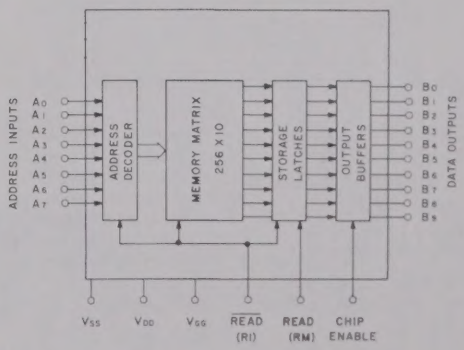
MK 2002 P / 2240-BIT ROM CHARACTER GENERATOR

- 64x5x7 organization
- ASCII-encoded
- Column output (7-bit)
- External column select
- 64 characters, 10x7 font size available using MK 2000 P pair
- Power supply: +14V; −14V
- Package: 28-pin CDIP



MK 2302 P / 2240-BIT ROM CHARACTER GENERATOR

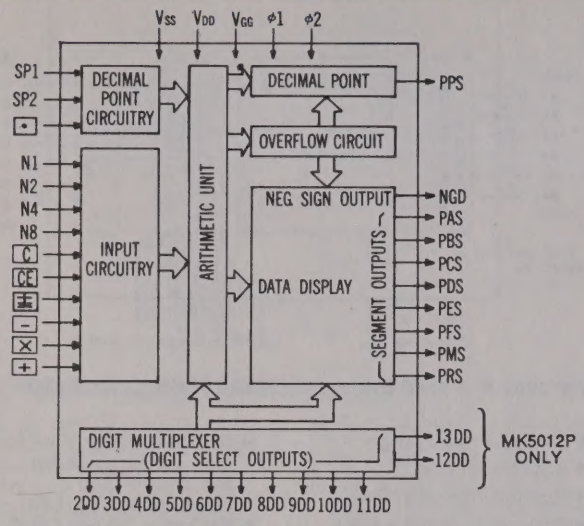
- 64x5x7 organization
- ASCII-encoded
- Column output (7-bit)
- 64 characters, 10x7 font size available using MK 2300 P pair
- Ion-implanted for full TTL/DTL compatibility
- Power supply: +5V; −12V
- Package: 24-pin CDIP



MK 2408 P / 2560-BIT ROM CHARACTER GENERATOR

- Row-out (5-bit); outputs 2 rows at a time
- 64 characters
- Ion-implanted for full TTL/DTL compatibility
- ASCII-encoded
- 550 ns cycle time
- Power supply: +5V, −12V
- Package: 28-pin CDIP

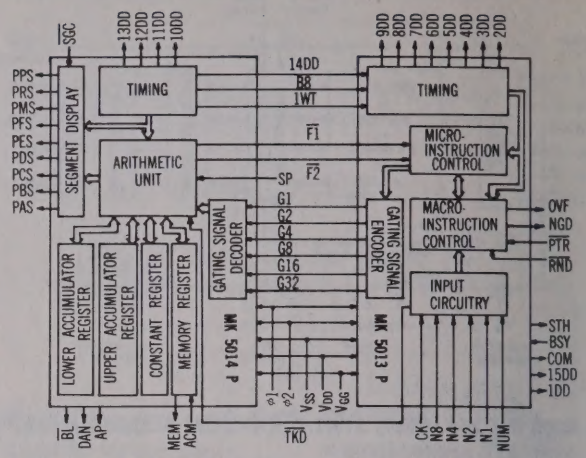
CALCULATORS



MK 5010 P / MK 5012 P

FOUR-FUNCTION SINGLE-CHIP CALCULATORS

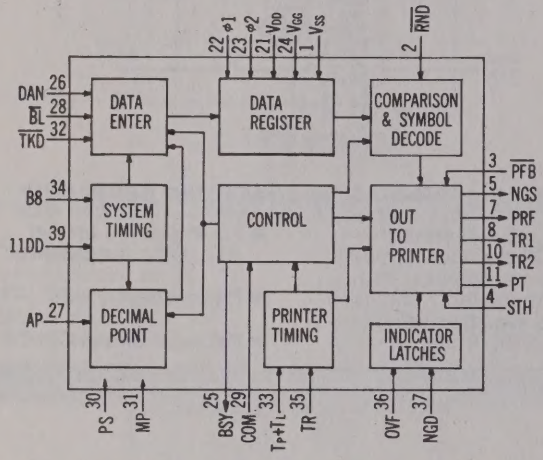
- Four-function (+, −, ×, ÷)
- MK 5010-P: 10 digit; MK 5012 P, 12-digit
- Selectable decimal placement
- Leading-zero blanking
- Overflow indication
- Negative sign indicator
- Chain calculations
- Power Supply: −8V, −13V
- Package: 40-pin CDIP



MK 5013 P & MK 5014 P

FOUR-FUNCTION CALCULATOR PAIR WITH MEMORY

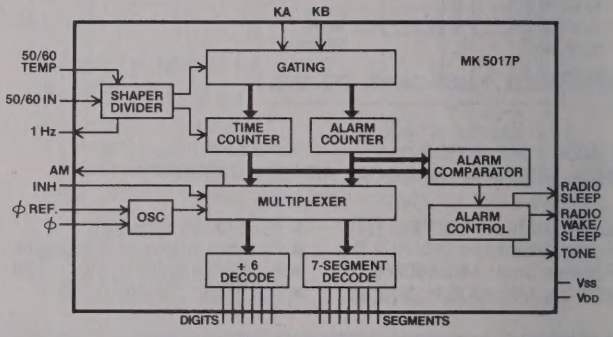
- Four-function (+, −, ×, ÷)
- 12-digit
- Floating point entry
- Fixed or floating point results
- Leading-zero blanking
- Indicators for:
  - Overflow
  - Negative sign
  - Memory in use
- Memory and other registers protected against overflow
- Automatic constant
- Selectable truncate or 5/4 round-off
- Register exchange capability
- Power supply: −8V, −13V
- Package: 40-pin CDIP



MK 5015 P / *PRINTING CALCULATOR INTERFACE*

- Interfaces MK 5013 P & MK 5014 P to printer
- Direct connection between chips — no buffering
- Designed for use with Seiko 102 drum printer
- Acts on coincidence to provide hammer-driver signal
- Provides function mnemonic printout
- Provides paper-feed information
- Provides ribbon-position information for two-color printout and carbon copies
- Power supply: −8V, −13V
- Package: 40-pin CDIP

CLOCKS



MK 5017 P/*PROGRAMMABLE DIGITAL CLOCK*

- Three versions now available
  - 5017 AA—Alarm Clock
  - 5017 AN—Clock Radio
  - 5017 BB—Calendar Clock
- Can be custom-microprogrammed for other timing/clock needs
- 4 or 6 digit operation — HRS, MINS, SECS
- 24 hour alarm with "snooze" feature
- 50/60 Hz line frequency operation
- 12/24 Hr. operation
- High current outputs for easy display interface
- Easy to set time or alarm
- Alarm tone generated on-chip
- Operation from single, 11V to 18V supply
- 24 or 28 pin CDIP

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MOS Shift Registers

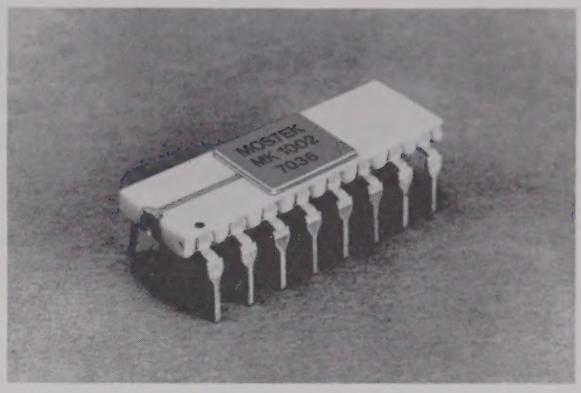
MOSTEK CORPORATION

DUAL 128-BIT

MOS Static Shift Register

MOSTEK

DS-100287I-3/FEB. 73



FEATURES

- ☐ Ion-implanted for full TTL/DTL compatibility — no interface circuitry required
- ☐ Single-phase, TTL/DTL compatible clocks
- ☐ Dual 128-bit static shift registers — 256 bits total
- ☐ Dual sections have independent clocks
- ☐ Recirculate logic built in
- ☐ DC to 1 MHz clock rates
- ☐ Low power dissipation — 130 mW
- ☐ 16-pin dual-in-line package

APPLICATIONS

- ☐ Delay lines
- ☐ Buffer data storage
- ☐ Recycling test data sequencer
- ☐ Digital filtering

DESCRIPTION

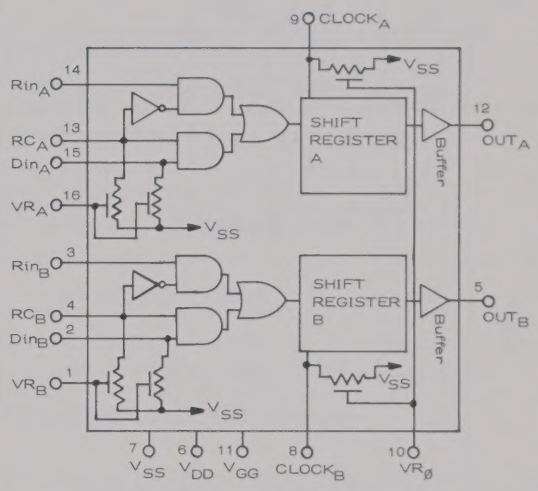
The MK 1002 P is a P-channel MOS static shift register utilizing low threshold-voltage processing and ion-implantation to achieve full TTL/DTL compatibility. Each of the two independent 128 bit sections has a built-in clock generator to generate three internal clock phases from a single-phase TTL-level external input. In addition, each section has input logic for loading or recirculating data within the register. (See Functional Diagram.) The positive-logic Boolean expression for this action is:

$$\text{OUT (delayed 128 bits)} = (R_C)(D_{in}) + (\overline{R_C})(R_{in})$$

The Data, Recirculate Control, and Clock inputs are provided with internal pull-up resistors to V_{SS} (+5V) for use when driving from TTL. These resistors can be disabled when driving from circuitry with larger output-voltage swings, such as DTL. Enabling of pull-up resistors is accomplished by connecting the appropriate terminal to V_{GG}; disabling by connecting to V_{SS}. The Recirculate inputs are not provided with pull-up resistors since they are generally driven from MOS.

Shifting data into the register is accomplished while the Clock input is low. Output data appears following the positive-going Clock edge. Data in each register can be held indefinitely by maintaining the Clock input high.

FUNCTIONAL DIAGRAM



OPERATING NOTES

R_C	R_{in}	D_{in}	DATA ENTERED
1	X	1	1
1	X	0	0
0	1	X	1
0	0	X	0

"1" = V_{SS} = +5V

"0" = V_{DD} = Grd

X = No Effect

Output Logic: See Description.

1215 W. Crosby Road, Carrollton, Texas 75006

MOSTEK®

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} . . . . . V_{SS} — 10.0 V
Supply Voltage, V_{GG} . . . . . V_{SS} — 20.0 V
Voltage at any Input or Output . . . . . V_{SS} + 0.3 V to V_{SS} — 10.0 V
Operating Free-air Temperature Range . . . . . 0°C to +75°C
Storage Temperature Range . . . . . —55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply Voltage	4.75	5.0	5.25	V	$V_{DD} = 0$ V
	V_{GG}	Supply Voltage[1]	—12.6	—12.0	—11.4	V	
INPUTS	V_{IL}	Input Voltage, Logic 0[2]		0	V_{SS}—4	V	
	V_{IH}	Input Voltage, Logic 1	V_{SS}—1	5.0		V	
INPUT TIMING	f	Clock Repetition Rate	DC		1	MHz	
	$t_{\phi p}$	Clock Pulse Width	0.35		10	μs	
	$t_{\phi d}$	Clock Pulse Delay	0.4			μs	See
	$t_{\phi r}$	Clock Pulse Risetime	.010		0.2	μs	Timing
	$t_{\phi f}$	Clock Pulse Falltime	.010		0.2	μs	Diagram
	t_{dId}	Data Leadtime	50			ns	
	t_{dIg}	Data Lagtime	200			ns	
	t_{rId}	Recirculate Control Leadtime	100			ns	
	t_{rIg}	Recirculate Control Lagtime	300			ns	

ELECTRICAL CHARACTERISTICS

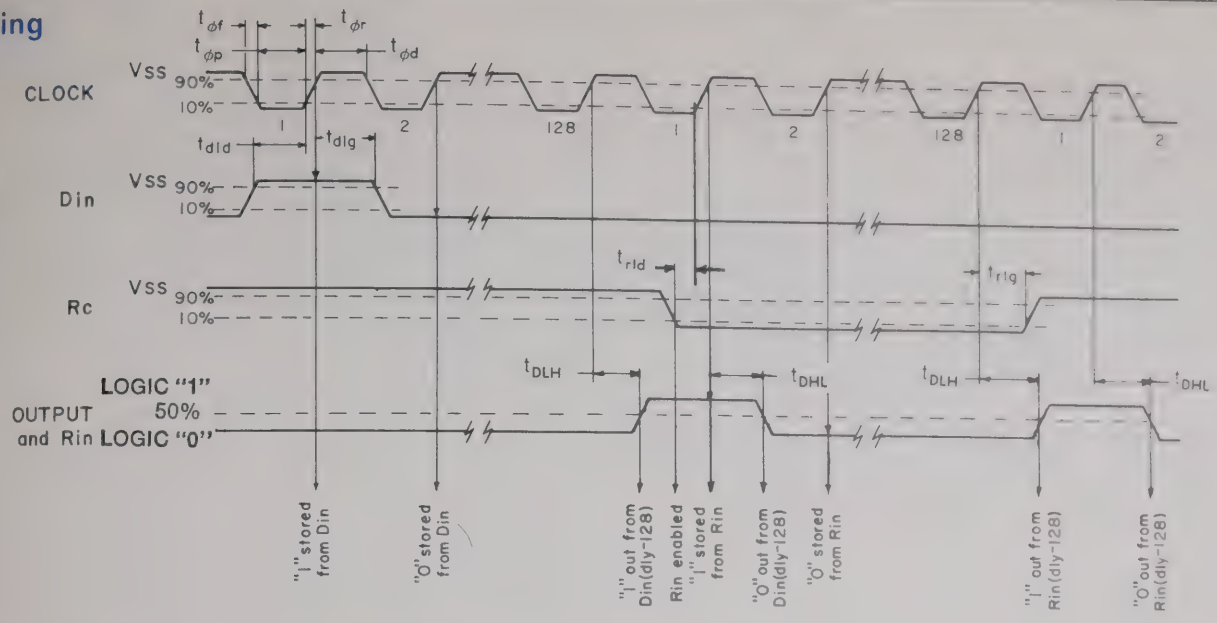
($V_{SS} = +5 \pm 0.25$V, $V_{GG} = -12 \pm 0.6$V, $T_A = 0°C$ to $+75°C$, using test circuit shown, unless otherwise noted.)

		PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Power Supply Current, V_{SS}		14	25	mA	$f_\phi = 1$ MHz Inputs & Outputs open
	I_{GG}	Power Supply Current, V_{GG}		5	10	mA	
INPUTS	C_i	Input Capacitance, any Input		3	10	pF	$V_I = V_{SS}$, f = 1 MHz $T_A = 25°C$
	I_{IL}	Input Current, Logic 0: Resistors Disabled[2]			−40	μA	$V_I = V_{SS} - 5$V
		Resistors Enabled[2]	−0.3		−1.6	mA	$V_I = +0.4$V
	I_{IH}	Input Current, Logic 1, Any Input			40	μA	VR_A, VR_B, $VR\phi = V_{SS}$ $V_I = V_{SS}$
	$I_{IR(on)}$	Input Current at Recirculate Inputs[2]			−40	μA	VR_A, VR_B, $VR\phi = V_{GG}$ $V_I = V_{SS} - 5$V
OUTPUTS	V_{OL}	Output Voltage, Logic 0 (3)			0.4	V	$I_L = -1.6$ mA
	V_{OH}	Output Voltage, Logic 1 (3)	$V_{SS} - 1$			V	$I_L = +100$ μA
DYNAMIC CHAR.	t_{DLH}	Output Delay, Low to High			450	ns	See Timing Diagram and Test Circuit $T_A = 25°C$
	t_{DHL}	Output Delay, High to Low			450	ns	
	t_{VOR}	Output Voltage Rise Time		100	150	ns	
	t_{VOF}	Output Voltage Fall Time		100	150	ns	

NOTES:

1. Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., $V_{SS} = 0$V, $V_{DD} = -5 \pm 0.25$V, $V_{GG} = -17 \pm 0.85$V.
2. MOS pull-up resistors to +5V are provided internally. These MOS resistors are enabled by connecting VR_A, VR_B and $VR\phi$ to V_{GG}, and disabled by connecting VR_A, VR_B and $VR\phi$ to V_{SS}. Pull-up resistors not provided at recirculate inputs.
3. At $T_A = 25°C$.

timing



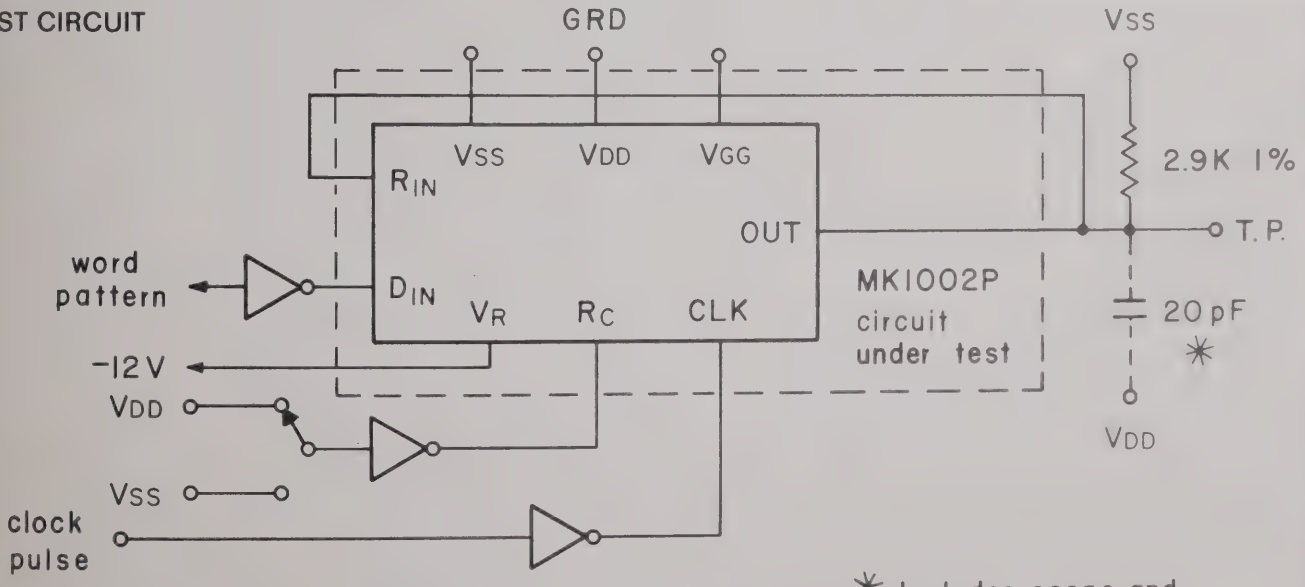
The timing diagram applies to either section of the dual shift register. The test conditions for these waveforms are illustrated below. A logic "1" is defined as +5 V and a logic "0" is defined as 0V

As long as R_C is at a "1", R_{in} is disabled and D_{in} is enabled. The data that is present at D_{in} while the clock is at "0" is shifted in and will be stored as the clock goes to a "1" This data must have been present t_{did} time prior to the clock "1" edge. The data must also remain in that same state for t_{dlg} time after that edge. These times are necessary to insure proper data storage in the first register-cell.

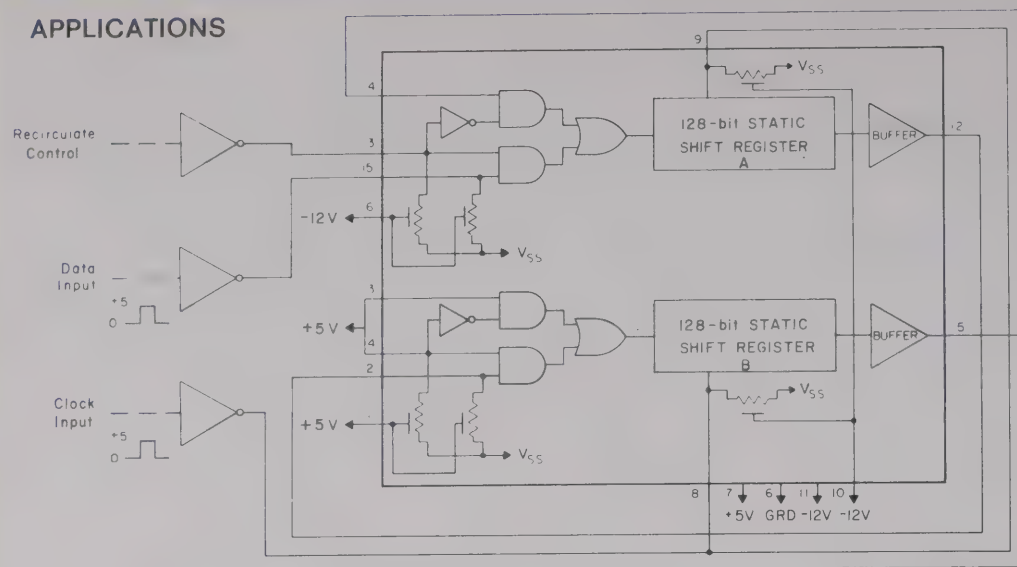
On the clock "1" edge, data is shifted through the register causing bit 127 to be shifted to position 128. This cell's output is buffered and appears at the output in the same logic polarity that appeared at the input 128 clocks prior. This data appears within t_{pd} time of the clock "1" edge.

R_{in} may be hardwired to the data output. When R_C is at a "0", R_{in} is enabled and D_{in} is disabled. Therefore, the output data will appear at the input of the first cell. When R_{in} is tied to the data output, the output delay will insure t_{dlg} and t_{did} times. R_C "0" time must lead the clock "1" edge by t_{rld} time and must lag that edge by t_{rlg} time to insure proper data storage when recirculate storage is desired.

TEST CIRCUIT



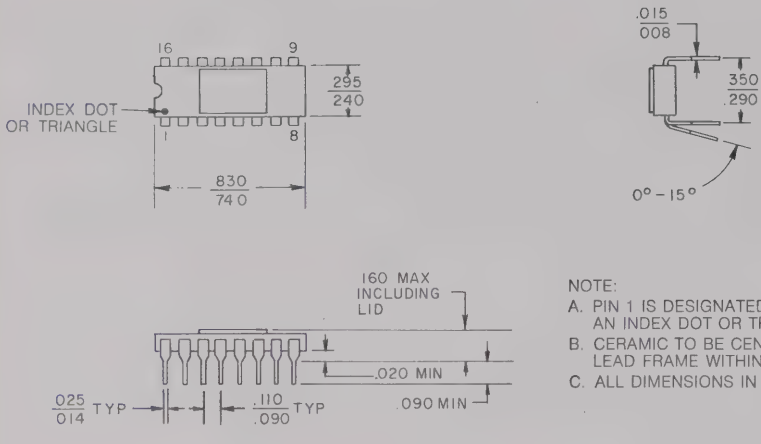
APPLICATIONS



This shows the MK 1002 P connected to operate as a single, 256-bit, static shift register. Pull-up resistors are enabled at TTL driven inputs and disabled at MOS or DTL driven inputs. Any similar TTL/DTL device may be used in place of the inverters shown.

Inverters are 74-series TTL

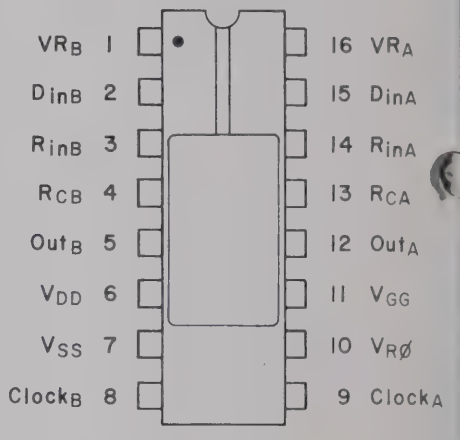
PACKAGE (16 Lead Ceramic Dual-In-Line Hermetic Package)



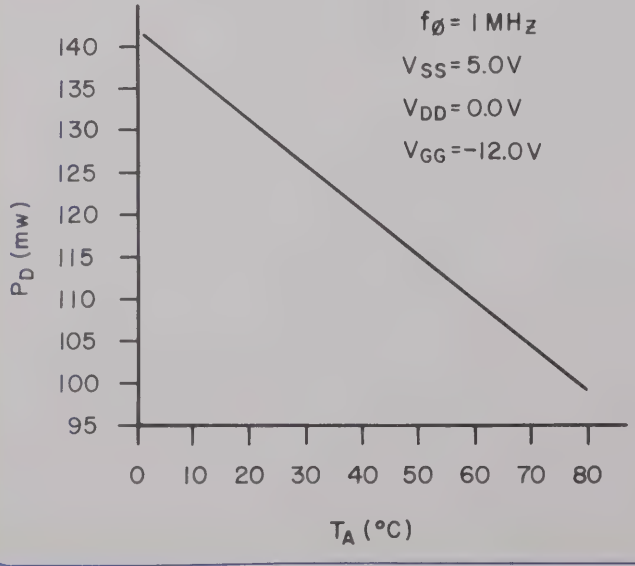
NOTE:
A. PIN 1 IS DESIGNATED BY AN INDEX DOT OR TRIANGLE
B. CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN .020"
C. ALL DIMENSIONS IN INCHES

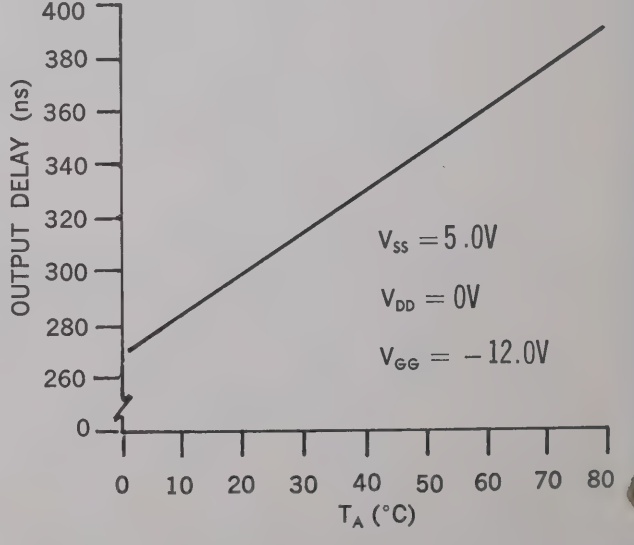
PIN CONNECTIONS

TOP VIEW
16 PIN CDIP



TYPICAL PERFORMANCE





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MK 1002 L

DS-1002L1070-3/FEB. 73

DUAL 128 BIT
MOS Static Shift Register

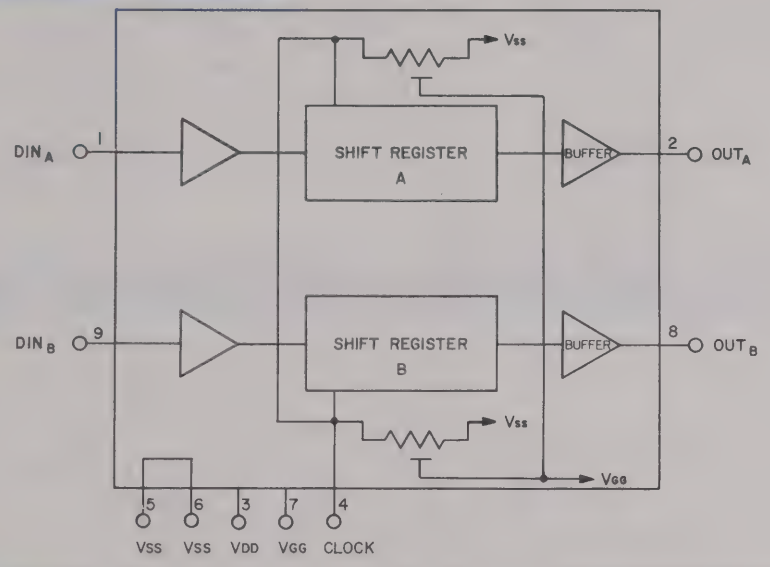
MOSTEK

DESCRIPTION

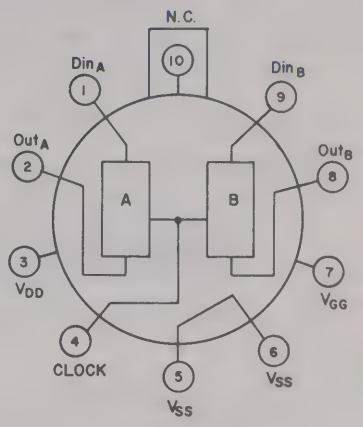
The MK 1002 is a P-channel MOS static shift register utilizing ion implant, low-threshold voltage processing to achieve full TTL/DTL compatibility. Each of the two independent 128-bit sections has a built-in clock generator to generate three internal clock phases from a single-phase TTL level external input.

Shifting data into the register is accomplished while the clock input is low. Output data appears following the positive-going clock edge. Data in each register can be held indefinitely by maintaining the clock input high.

FUNCTIONAL DIAGRAM



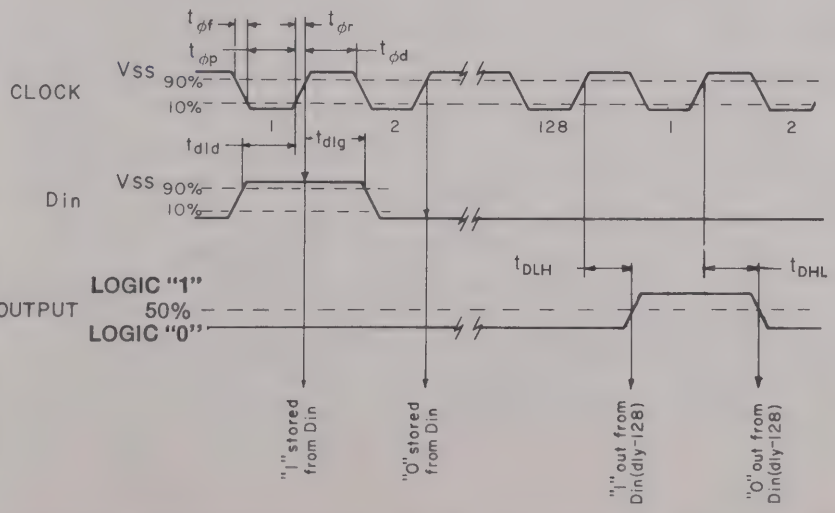
PIN CONNECTIONS



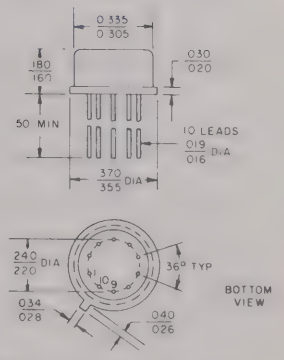
TOP VIEW

N.C. = no connection

TIMING



PACKAGE



NOTES

A ALL DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED

B ALL LEADS WELDABLE AND SOLDERABLE

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MOSTEK®

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	V_{SS} — 10.0 V
Supply Voltage, V_{GG}	V_{SS} — 20.0 V
Voltage at any Input or Output	V_{SS} + 0.3 V to V_{SS} — 10.0 V
Operating Free-air Temperature Range	0°C to +75°C
Storage Temperature Range	—55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply Voltage	4.75	5.0	5.25	V	$V_{DD} = 0$ V
	V_{GG}	Supply Voltage[1]	—12.6	—12.0	—11.4	V	
INPUTS	V_{IL}	Input Voltage, Logic 0[2]		0	V_{SS}—4	V	
	V_{IH}	Input Voltage, Logic 1	V_{SS}—1	5.0		V	
INPUT TIMING	f_ϕ	Clock Repetition Rate	DC		1	MHz	
	$t_{\phi P}$	Clock Pulse Width	0.35		10	μs	
	$t_{\phi d}$	Clock Pulse Delay	0.4			μs	See
	$t_{\phi r}$	Clock Pulse Risetime	.010		0.2	μs	Timing
	$t_{\phi f}$	Clock Pulse Falltime	.010		0.2	μs	Diagram
	t_{dld}	Data Leadtime	50			ns	
	t_{dlg}	Data Lagtime	200			ns	

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5 \pm 0.25V, V_{GG} = -12 \pm 0.6V, T_A = 0°C$ to $+75°C$, unless otherwise noted.)

		PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Power Supply Current, V_{SS}		14	25	mA	$f_\phi = 1$ MHz Inputs & Outputs open
	I_{GG}	Power Supply Current, V_{GG}		5	10	mA	
INPUTS	C_i	Input Capacitance, any Input		6	10	pF	$V_I = V_{SS}$, f = 1 MHz
		Clock		12	20	pF	$T_A = 25°C$
	I_{IL}	Input Current, Logic 0, Data			—40	μA	$V_I = V_{SS}$ —5V
		Clock	-0.6		—3.2	mA	$V_I = +0.4V$
	I_{IH}	Input Current, Logic 1, Any Input			40	μA	$V_I = V_{SS}$
OUTPUTS	V_{OL}	Output Voltage, Logic 0			0.4	V	$I_L = -1.6$ mA
	V_{OH}	Output Voltage, Logic 1	$V_{SS} - 1$			V	$I_L = +100\ \mu$A $T_A = 25°C$
DYNAMIC CHAR.	t_{DLH}	Output Delay, Low to High			450	ns	
	t_{DHL}	Output Delay, High to Low			450	ns	See Timing
	t_{VOR}	Output Voltage Rise Time		100	150	ns	Diagram $T_A = 25°C$
	t_{VOF}	Output Voltage Fall Time		100	150	ns	

NOTES:

1. Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., $V_{SS} = 0V$, $V_{DD} = -5 \pm 0.25V$, $V_{GG} = -17 \pm 0.85V$.
2. Pull-up resistances to +5V are provided internally at Clock Input.
3. All typical values at $T_A = 25°C$.

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MK 1002 L

DS-1002L1070-3/FEB. 73

DUAL 128 BIT
MOS Static Shift Register

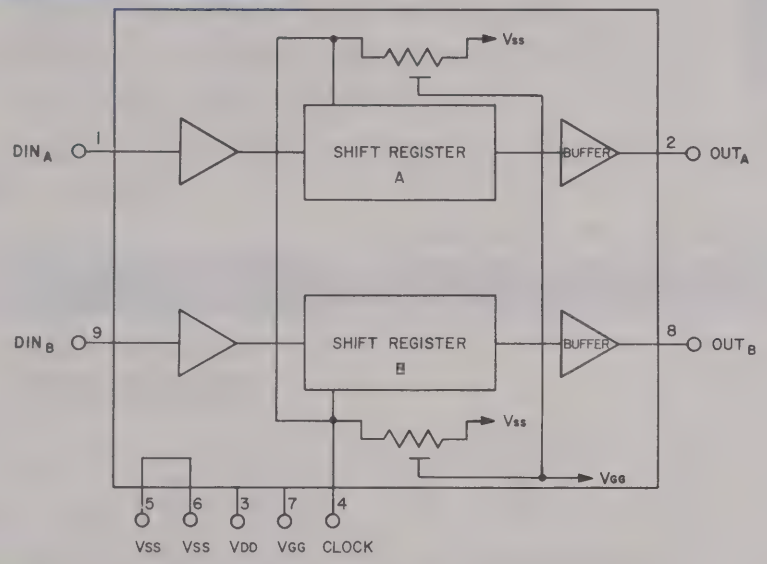
MOSTEK

DESCRIPTION

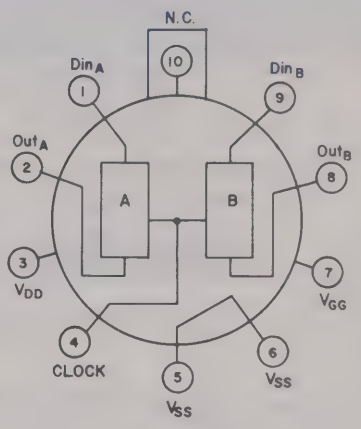
The MK 1002 is a P-channel MOS static shift register utilizing ion implant, low-threshold voltage processing to achieve full TTL/DTL compatibility. Each of the two independent 128-bit sections has a built-in clock generator to generate three internal clock phases from a single-phase TTL level external input.

Shifting data into the register is accomplished while the clock input is low. Output data appears following the positive-going clock edge. Data in each register can be held indefinitely by maintaining the clock input high.

FUNCTIONAL DIAGRAM



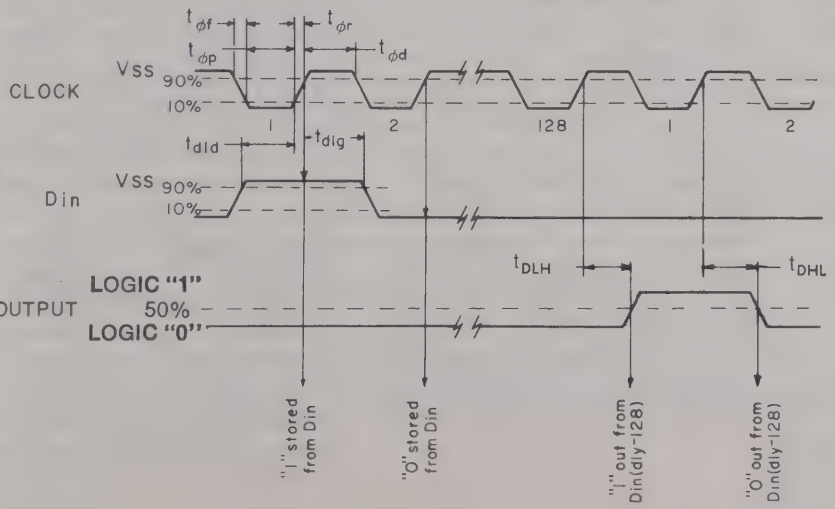
PIN CONNECTIONS



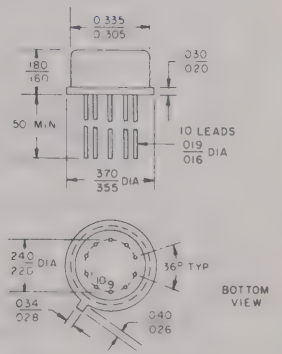
TOP VIEW

N.C. = no connection

TIMING



PACKAGE



NOTES

A ALL DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED

B ALL LEADS WELDABLE AND SOLDERABLE

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MOSTEK®

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	V_{SS} — 10.0 V
Supply Voltage, V_{GG}	V_{SS} — 20.0 V
Voltage at any Input or Output	V_{SS} + 0.3 V to V_{SS} — 10.0 V
Operating Free-air Temperature Range	0°C to +75°C
Storage Temperature Range	—55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply Voltage	4.75	5.0	5.25	V	$V_{DD} = 0$ V
	V_{GG}	Supply Voltage[1]	—12.6	—12.0	—11.4	V	
INPUTS	V_{IL}	Input Voltage, Logic 0[2]		0	V_{SS}—4	V	
	V_{IH}	Input Voltage, Logic 1	V_{SS}—1	5.0		V	
INPUT TIMING	f_ϕ	Clock Repetition Rate	DC		1	MHz	
	$t_{\phi P}$	Clock Pulse Width	0.35		10	μs	
	$t_{\phi d}$	Clock Pulse Delay	0.4			μs	See
	$t_{\phi r}$	Clock Pulse Risetime	.010		0.2	μs	Timing
	$t_{\phi f}$	Clock Pulse Falltime	.010		0.2	μs	Diagram
	t_{dld}	Data Leadtime	50			ns	
	t_{dlg}	Data Lagtime	200			ns	

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5 \pm 0.25V, V_{GG} = -12 \pm 0.6V, T_A = 0°C$ to $+75°C$, unless otherwise noted.)

		PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Power Supply Current, V_{SS}		14	25	mA	$f_\phi = 1$ MHz Inputs & Outputs open
	I_{GG}	Power Supply Current, V_{GG}		5	10	mA	
INPUTS	C_i	Input Capacitance, any Input		6	10	pF	$V_I = V_{SS}$, f = 1 MHz
		Clock		12	20	pF	$T_A = 25°C$
	I_{IL}	Input Current, Logic 0, Data			−40	μA	$V_I = V_{SS}$ —5V
		Clock	-0.6		−3.2	mA	$V_I = +0.4V$
	I_{IH}	Input Current, Logic 1, Any Input			40	μA	$V_I = V_{SS}$
OUTPUTS	V_{OL}	Output Voltage, Logic 0			0.4	V	$I_L = -1.6$ mA
	V_{OH}	Output Voltage, Logic 1	$V_{SS} - 1$			V	$I_L = +100$ μA $T_A = 25°C$
DYNAMIC CHAR.	t_{DLH}	Output Delay, Low to High			450	ns	
	t_{DHL}	Output Delay, High to Low			450	ns	See Timing
	t_{VOR}	Output Voltage Rise Time		100	150	ns	Diagram $T_A = 25°C$
	t_{VOF}	Output Voltage Fall Time		100	150	ns	

NOTES:

1. Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., $V_{SS} = 0V$, $V_{DD} = -5 \pm 0.25V$, $V_{GG} = -17 \pm 0.85V$.
2. Pull-up resistances to +5V are provided internally at Clock Input.
3. All typical values at $T_A = 25°C$.

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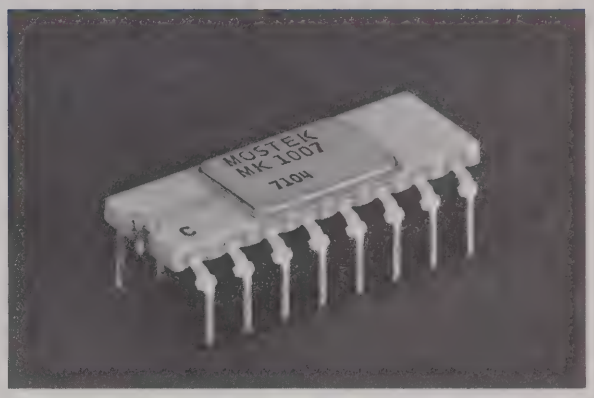
MK 1007 P

DS-1007571-3/JULY 1972

320 Bits (4x80)

MOS Dynamic Shift Register

MOSTEK CORPORATION



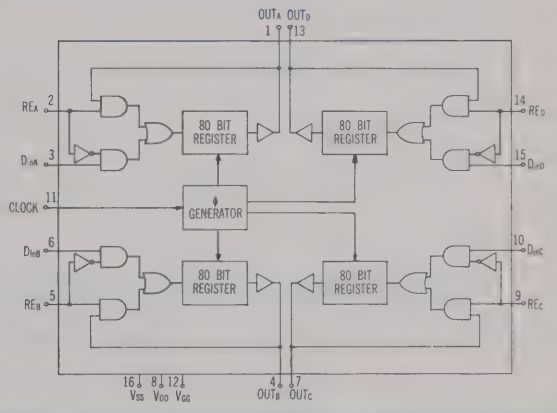
FEATURES:

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Single-phase, TTL/DTL-compatible clock
- ☐ Internal pull-up resistors
- ☐ Clock frequency 10 kHz to 2.5 MHz
- ☐ Built-in recirculate logic for each register
- ☐ Power Supplies: +5V and −12V

APPLICATIONS:

- ☐ CRT display systems
- ☐ Buffer data storage
- ☐ Delay lines
- ☐ Digital filtering

FUNCTIONAL DIAGRAM



DESCRIPTION

The MK 1007 P contains four separate 80-bit MOS dynamic shift registers on a single chip, using ion-implantation in conjunction with P-channel processing to achieve low threshold voltage and direct TTL/DTL compatibility. All logic inputs, including the single-phase Clock, can be driven directly from DTL or TTL logic. Pull-up resistors to +5V are provided for worst-case TTL inputs.

Each 80-bit register has independent inputs and outputs and a control input (RE) which allows external data to be shifted into the register (at logical 0) or data at the output to be recirculated into the register (at logical 1).

All four registers use a common (external) Clock input. With the Clock high (1), data is shifted into the registers. Following the negative-going edge of the Clock, data shifting is inhibited and output data appears. Output data is True, delayed 80 bits.

Since the MK 1007 P has zero lag-time requirements for data inputs, devices may be cascaded, i.e., the output of one device may be fed directly to the input of another device. All inputs are protected to prevent damage due to static charge accumulation.

OPERATING NOTES:

1. Recirculate Enable (RE) = Logic 1 = output data recirculated.
2. Output data (delayed 80 bits) maintains same logic state when RE = 1.
3. Recirculate Enable (RE) = Logic 0 = Data In (D_{in}) enabled.
4. Output data (delayed 80 bits) attains same logic state as D_{in} when RE = 0.
5. Output data follows the clock negative edge.

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MOSTEK CORPORATION ®

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD}	V_{SS} + 0.3 V to V_{SS} − 20 V
Supply Voltage V_{GG}	V_{SS} + 0.3 V to V_{SS} − 20 V
Voltage at any Input or Output	V_{SS} + 0.3 V to V_{SS} − 20 V
Operating Free-air Temperature Range	0°C to 75°C
Storage Temperature Range	−55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

(0°C ≤ T_A ≤ 75°C)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS} Supply Voltage	4.75	5.0	5.25	V	V_{DD} = 0 V
	V_{GG} Supply Voltage[1]	−12.6	−12.0	−11.4	V	
INPUTS	V_{IL} Logic "0" Voltage, any input		0.0	0.8	V	
	V_{IH} Logic "1" Voltage, any input [2]	V_{SS} − 1.5	+5.0		V	
INPUT TIMING	$f\phi$ Clock Repetition Rate	.01		2.5	MHz	
	$t\phi_p$ Clock Pulse Width	.150		100	μs	NOTE: Total permitted clock times will be determined by clock frequency, $f\phi$.
	$t\phi_d$ Clock Pulse Delay	.150		100	μs	
	$t\phi_r$ Clock Pulse Risetime	.010		5	μs	
	$t\phi_f$ Clock Pulse Falltime	.010		5	μs	
	t_{dld} Data Leadtime	150			ns	
	t_{dlg} Data Lagtime	0			ns	
	t_{rld} Recirculate Control Leadtime	200			ns	
	t_{rlg} Recirculate Control Lagtime	50			ns	

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5 ±0.25 V, V_{GG} = −12 ±0.6V, T_A = 0°C to +75°C, unless otherwise specified.)

	PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS} V_{SS} Power Supply Current[4]		22.0	40.0	mA	$f\phi$ = 2.5 MHz;
	I_{GG} V_{GG} Power Supply Current		9.0	16.0	mA	outputs open; T_A=25°C
INPUTS	C_{IN} Capacitance at Data, RE, and Clock Inputs		3	6	pF	V_I = V_{SS}, $f\phi$ = 1 MHz, T_A = 25°C.
	I_{IL} Logic "0" Current, any input	0.6	1.1	1.6	mA	V_I=0.4 V; T_A=25°C
	$I_{I(lk)}$ Leakage Current, any input			1	μA	V_I=V_{SS}−5.5V; V_{SS}=V_{DD}=V_{GG}
	R_{IN} Input Pullup Resistance	3.0		8.4	kΩ	V_I=0.4 V; T_A=25°C
OUTPUTS	V_{OL} Logic "0" Output Voltage			0.4	V	I_L = −1.6 mA ; T_A=25°C
	V_{OH} Logic "1" Output Voltage	V_{SS} − 1			V	I_L = +100 μA ; T_A=25°C
DYN. CHAR.	t_{DLH} Output Delay, Low to High		75	200	ns	See Timing Diagrams
	t_{DHL} Output Delay, High to Low		75	200	ns	
POWER DIS.	$P_{D(1)}$ Power Dissipation[4]		220		mW	$f\phi$ = 2.5 MHz
	$P_{D(2)}$ Power Dissipation[4]		195		mW	$f\phi$ = 1 MHz
	$P_{D(3)}$ Power Dissipation[4]		170		mW	$f\phi$ = 10 kHz

NOTES:

(1) Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., V_{SS}=0 V, V_{DD}= −5V, V_{GG}= −17 V.
(2) Pull-up resistances to +5V are provided internally.
(3) Typical values at T_A=25°C, V_{SS}=+5.0 V, V_{DD}=−12.0 V.
(4) I_{SS} will increase a maximum of 1.6 mA for each input at logic "0."

TIMING

CONDITIONS:

1. All timing relationships apply to any of the four registers.
2. Logic 0 is defined as V_{DD} or ground; logic 1 as V_{SS} or +5V.

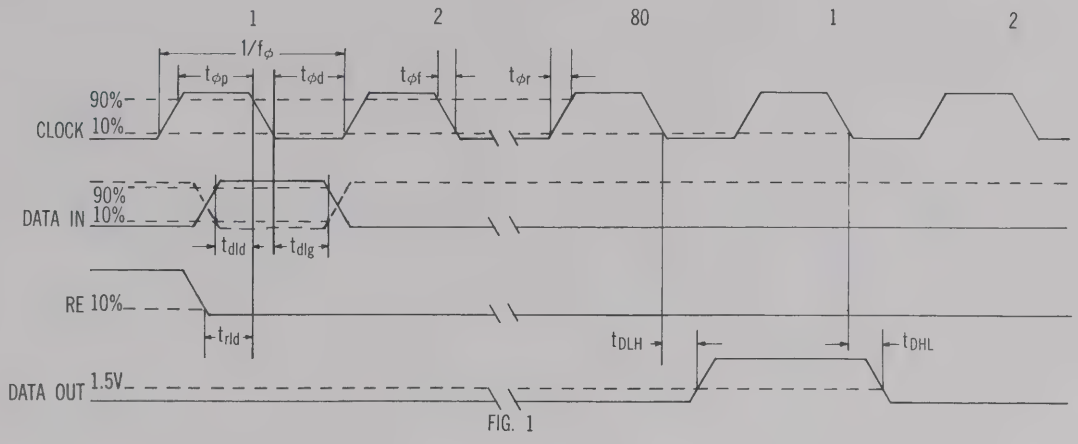


FIG. 1

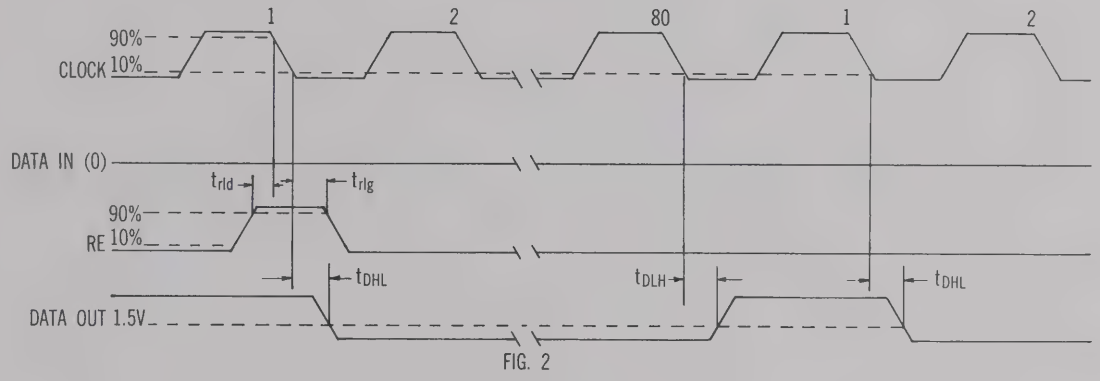


FIG. 2

SHIFT: Fig. 1 illustrates shifting a logic 1 bit from the Data Input (D_{in}) through one of the 80-bit registers. RE (Recirculate Enable) at logic 0 enables D_{in}. RE must go to logic 0 for t_{rld} time (Recirculate Control Leadtime) prior to the Clock's negative edge, and must maintain that state at least until the Clock's negative edge (t_{dlg}) to insure proper data shifting. This data bit entered will appear 80 clock pulses later within Output Delay Time (t_D) of that Clock's negative edge.

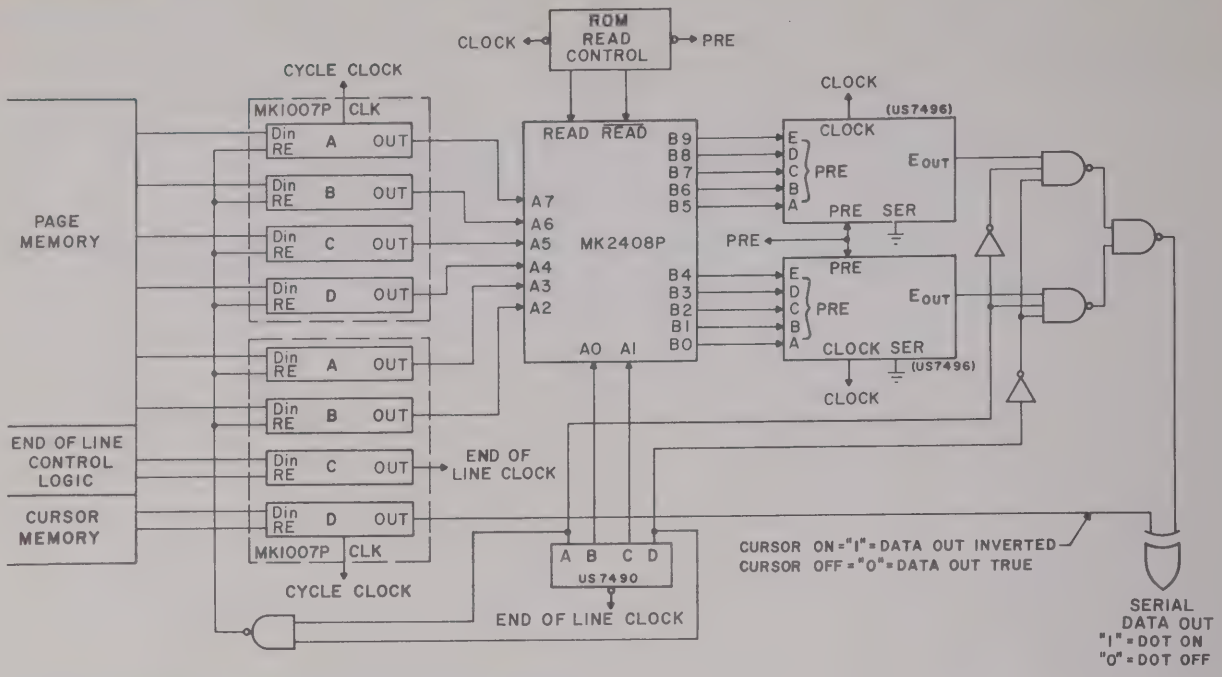
RECIRCULATE: Fig. 2 illustrates recirculating a bit present at the output back through the register. RE must attain a logic 1 for t_{rld} time (Recirculate Control Leadtime) prior to the Clock's negative edge, and must maintain that state at least until the Clock's negative edge (t_{rlg}) to insure proper data recirculation. The bit entered will appear 80 clocks later as shown.

MOSTEK CORPORATION

MK 1007 P

MOS Dynamic Shift Register

APPLICATIONS



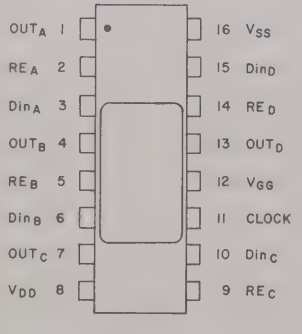
LINE REFRESH MEMORY FOR CRT DISPLAY

This application shows the MK 1007 P used as the Line Refresh Memory, driving MOSTEK's MK 2408 P TTL-compatible character generator. The MK 1007 P receives new data from the Page Memory (which may also consist of MK 1007 P's) on the tenth row of any character line, this being the third vertical space between rows of characters. The MK 1007 P recirculates the character-address data as these characters are scanned and displayed on a CRT screen.

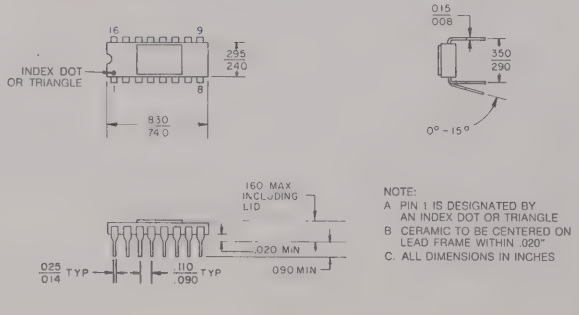
The decade counter selects the appropriate rows from the character generator which outputs two rows of the addressed character at one time (see MK 2408 P data sheet), and also controls the multiplexed output of the character generator so that only one row of the addressed characters is displayed on any CRT horizontal sweep.

One stage of the MK 1007 P may be used to shift a single data bit, which may be used to determine the end of the horizontal sweep. Another stage may be used as a cursor control and, as shown above, may blank the cursored character dots while surrounding dots are on, to give a reverse image of that particular character.

TOP VIEW
16 PIN CDIP

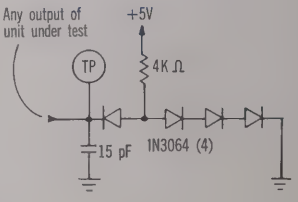


PACKAGE (16-lead ceramic dual-in-line hermetic package)



NOTE:
A. PIN 1 IS DESIGNATED BY AN INDEX DOT OR TRIANGLE
B. CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN .020"
C. ALL DIMENSIONS IN INCHES

TEST CIRCUIT



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MOS Read-Only Memories

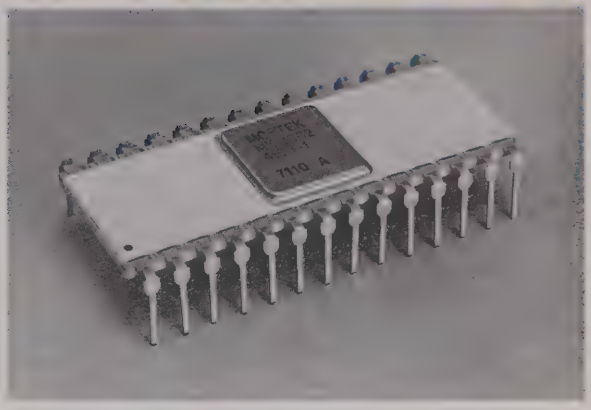
MOSTEK CORPORATION

MK 2000 P SERIES
MK 2002 P

DS-20001070-2/OCT. 1971

MOS Read-Only Memory Character Generators

MOSTEK



FEATURES

- 64 dot-matrix (5×7) characters with column-by-column output
- 32 dot-matrix (5×14) characters available as programming option
- High speed character access time and column select access time
- Completely static operation—no clocks required
- MK 2002 P is pre-programmed with ASCII encoding
- Easy interfacing to TTL/DTL
- Single mask custom programming

APPLICATIONS

- CRT alphanumeric displays
- Light-Emitting Diode (LED) array driver
- Billboard and stock market displays

DESCRIPTION

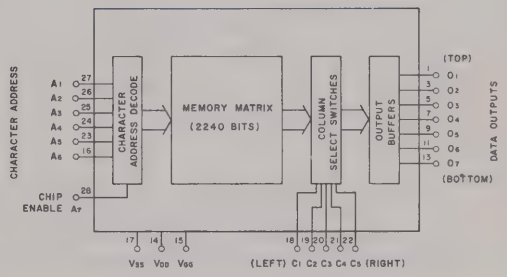
This MK 2000 P Series MOS Read-Only Memories (ROMs) is designed specifically for dot-matrix character generation where column-by-column data output is desired. Each ROM contains 2240 bits of programmable storage, organized as 64 characters, each having 5 columns of 7 bits. P-channel, enhancement-mode, MOS technology is employed in this series. All inputs are protected to prevent damage due to static charge accumulation.

Programming is accomplished during the manufacturing process by modification of a single mask in accordance with customer specifications. The MK 2002 P is pre-programmed with ASCII-encoded characters with the font shown on the back page.

In addition to the 64 character, 5 x 7 configuration, the MK 2000 P Series may also be programmed for 32 characters, each having 5 columns by 14 bits.

Memory operation is static and no refresh clocks are required to maintain output information. Character selection is achieved by presenting a seven-bit binary word at the address inputs. The most significant bit (A_7) is generally used as a Chip Enable. (See Operating Notes.) Column select lines, C_1 through C_5, select the column information that appears at the seven data outputs. (See Operating Notes.) By sequentially strobing C_1 through C_5, the font for the addressed character would be displayed. The output buffers are open-ended current sources, sourcing current from the V_{SS} supply only in the "dot-on" condition.

FUNCTIONAL DIAGRAM



OPERATING NOTES

"1" = V_{DD} "0" = V_{SS}						
A_7	C_1	C_2	C_3	C_4	C_5	Column Selected
0	X	X	X	X	X	None*
1	0	0	0	0	0	None*
1	1	0	0	0	0	1 (left)
1	0	1	0	0	0	2
1	0	0	1	0	0	3
1	0	0	0	1	0	4
1	0	0	0	0	1	5 (right)

X = No effect on columns
* Outputs open-circuited

1215 W. Crosby Road, Carrollton, Texas 75006

MOSTEK®

absolute maximum ratings

Voltage on any terminal relative to V_{SS} ..... +0.3V to −30V
Operating temperature range ..... −25°C to +85°C
Storage temperature range ..... −55°C to +150°C

recommended operating conditions

(−25°C≤T_A≤85°C)

	PARAMETER		MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage		0.0		V	
	V_{DD}	Supply voltage	−12.0	−14.0	−16.0	V	See note 1
	V_{GG}	Supply voltage	−24.0	−28.0	−29.0	V	
INPUTS	$V_{in(0)}$	Input voltage, logic "0"	V_{SS}−3	V_{SS}		V	
	$V_{in(1)}$	Input voltage, logic "1"		V_{DD}	V_{SS}−11	V	

electrical characteristics

(V_{SS}=0.0V; V_{DD}=−14.0V; V_{GG}=−28.0V, T_A=25°C unless noted otherwise)

	PARAMETER		MIN	TYP	MAX	UNITS	CONDITIONS
POWER	I_{DD}	Supply current (V_{DD})		13	25	mA	Outputs unconnected
	I_{GG}	Supply current (V_{GG})		1.5	3.0	mA	See note 2
INPUTS	C_{in}	Input capacitance			10	pF	V_{in}=V_{SS}, f_{meas}=1MHz
	I_{in}	Input leakage current			10	μA	V_{in}=V_{SS}−14V
OUTPUTS	V_{out}	Output voltage			V_{SS}−2	V	I_{out}=2.0 mA
					V_{SS}−5	V	I_{out}=4.0 mA
	$I_{out(on)}$	Output current, "dot-on"	6	12		mA	See Figure #3
	$I_{out(off)}$	Output current, "dot-off"			+10	μA	V_{out}=V_{SS}−14V
DYNAMIC CHARACTERISTICS	$t_{A(on)}$	Character access time, I_{off} to I_{on}		320	700	ns	V_{DD}=−14V, V_{GG}=−28V
				380	700	ns	V_{DD}=−12, V_{GG}=−24V
	$t_{A(off)}$	Character access time, I_{on} to I_{off}		190	700	ns	V_{DD}=−14V, V_{GG}=−28V
				220	700	ns	V_{DD}=−12V, V_{GG}=−24V
	$t_{C(on)}$	Column select delay time, I_{off} to I_{on}		90	250	ns	V_{DD}=−14V, V_{GG}=−28V
				95	300	ns	V_{DD}=−12V, V_{GG}=−24V
	$t_{C(off)}$	Column select delay time, I_{on} to I_{off}		180	250	ns	V_{DD}=−14V, V_{GG}=−28V
				205	300	ns	V_{DD}=−12V, V_{GG}=−24V
	t_{OE}	Output enable/disable delay time		320	700	ns	V_{DD}=−14V, V_{GG}=−28V
	t_{AV}	Character access time (V_{out})		500		ns	V_{SS}=+14V, V_{DD}=0V, V_{GG}=−14V

See Figures #1, #2 and Timing

See Figure #1 and Timing

See Figure #4 and Timing

NOTES: 1. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., V_{SS} = +14.0V, V_{DD} = 0.0V, V_{GG} = −14.0V.
2. I_{SS}=I_{DD}+I_{GG}

timing

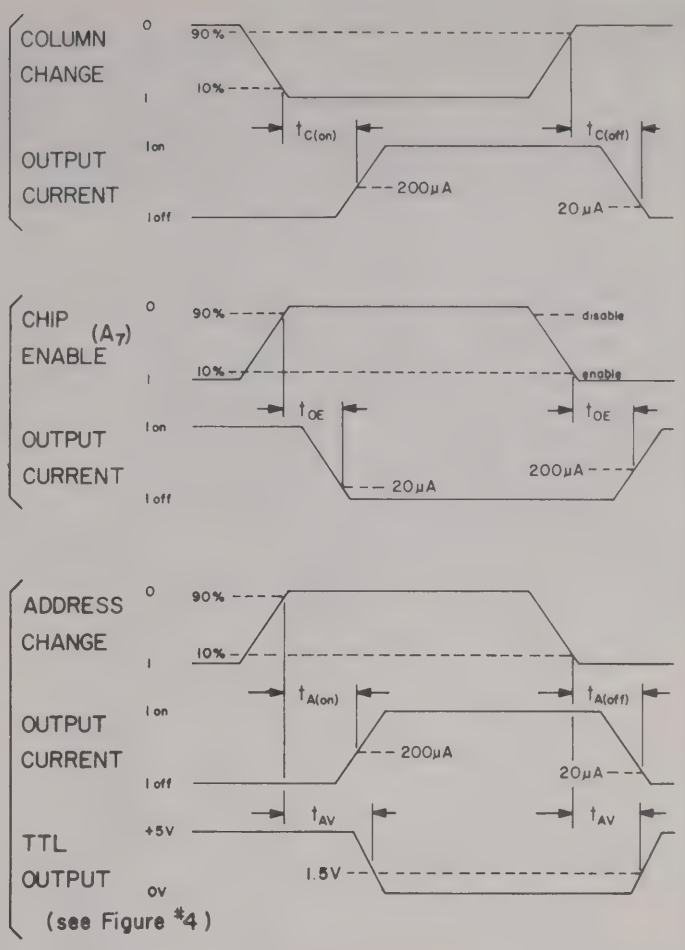
(waveforms not to scale)

The A_7 input on The MK 2000 P Series may be programmed as a seventh address bit or as a chip enable, in which case either logic level may be chosen to enable the circuit.

When the A_7 input on The MK 2002 P is at a logical "O" (V_{SS}), the output buffers are turned off (I_{off}). When re-enabled, the chip will respond to the address and column selected at that time.

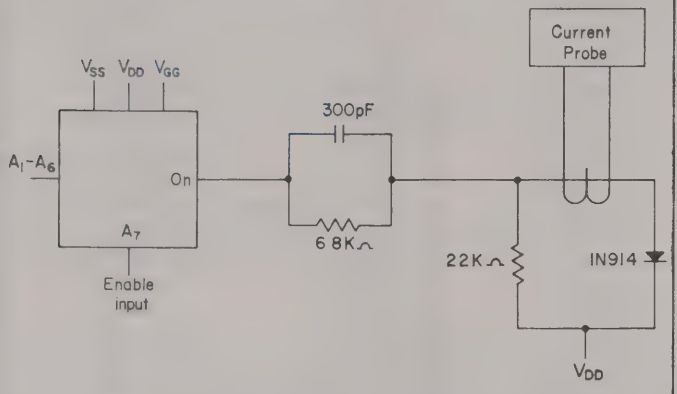
Columns are selected by applying a logical "1" (V_{DD}) to the appropriate select line while the other four select lines are at "0". Column selection may change while the address is held constant or addresses may be changed while any column is selected, or both may be changed simultaneously.

The MK 2000 P Series output buffers source current from the V_{SS} supply as indicated in Figure 3. Figure 4 is a suggested TTL/DTL interface. Delay time, t_{AV}, is measured to the output of the TTL shown in Figure 4.



test circuit

FIGURE #1



typical performance

FIGURE #2

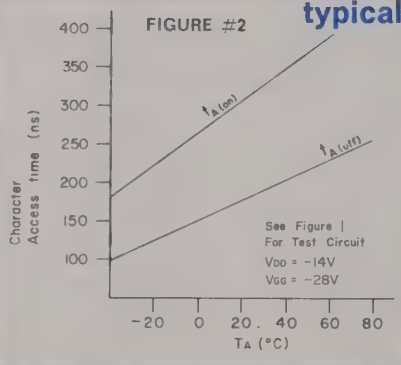
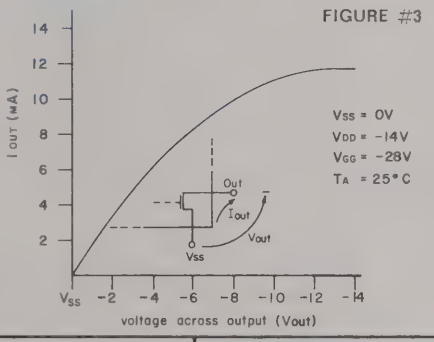
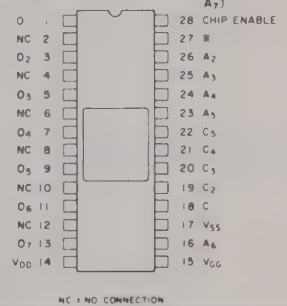


FIGURE #3



pin connections

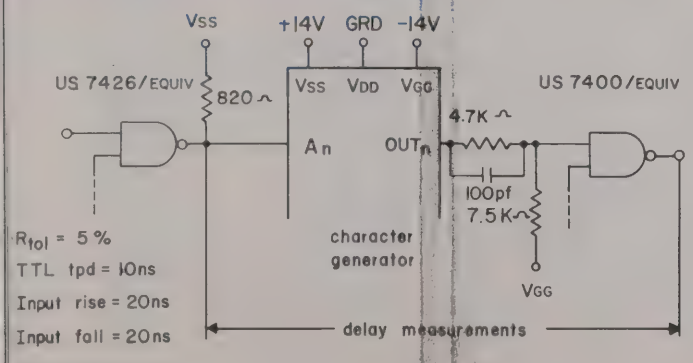
Top View, 28 Pin CDIP



NC = NO CONNECTION

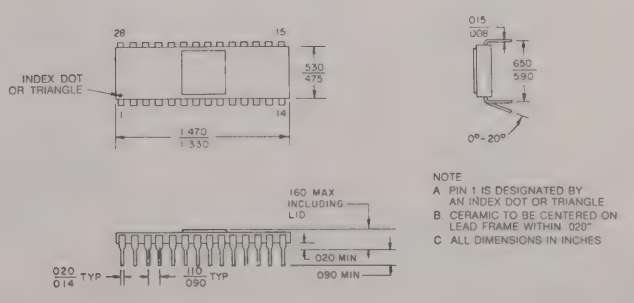
interface diagram/test circuit

FIGURE #4



physical description

(28 lead ceramic dual-in-line hermetic package)

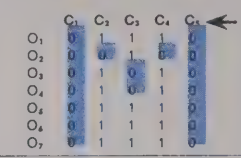


NOTE
A. PIN 1 IS DESIGNATED BY AN INDEX DOT OR TRIANGLE
B. CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN .020"
C. ALL DIMENSIONS IN INCHES

coding and character fonts

The MK 2002 P is a pre-programmed member of the MK 2000 P Series with ASCII encoding and the character fonts shown below. A logic "0" represents an input voltage equal to V_{SS}, or an output I_{ON}, and a logic "1" represents a voltage equal to V_{DD}, or an output I_{off}.

An example demonstrating the correspondence of device outputs and sequence to the 5 x 7 dot matrix fonts is shown below:



MK 2002 P				A_6	1	1	0	0
				A_5	0	1	0	1
A_4	A_3	A_2	A_1	COL / ROW	2	3	4	5
0	0	0	0	0				
0	0	0	1	1				
0	0	1	0	2				
0	0	1	1	3				
0	1	0	0	4				
0	1	0	1	5				
0	1	1	0	6				
0	1	1	1	7				
1	0	0	0	8				
1	0	0	1	9				
1	0	1	0	10				
1	0	1	1	11				
1	1	0	0	12				
1	1	0	1	13				
1	1	1	0	14				
1	1	1	1	15				

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MK 2300 P SERIES
MK 2302 P

2240 BIT
MOS Read-Only Memory Character Generators

MOSTEK

DS-2300670-2/DEC. 1971

FEATURES

- ☐ Ion-implantation processing for full TTL/DTL compatibility
- ☐ 2240 bits of storage organized as 64 5x7 dot matrix characters with column-by-column output
- ☐ 7x10 row-by-row, 64-character output capability available
- ☐ MK 2302 P is pre-programmed with ASCII encoding
- ☐ Internal counter provides clocked column selection
- ☐ Counter output for updating external character address registers
- ☐ Internal provision for one- or two-column intercharacter spacing
- ☐ Output enable and blanking capability
- ☐ Operates from +5V and —12V supplies

APPLICATIONS

- ☐ CRT alphanumeric displays
- ☐ Light-Emitting Diode (LED) array driver
- ☐ Billboard and stock market displays

DESCRIPTION

The MK 2300 P Series MOS, TTL / DTL-compatible read-only memories (ROMs) are designed specifically for dot-matrix character generation. Each ROM provides 2240 bits of programmable storage, organized as 64 characters each having 5 columns of 7 bits. A row output capability for 64 7x10 characters is available, as illustrated on the back page.

Low threshold-voltage processing, utilizing ion-implantation, is used with P-channel, enhancement-mode MOS technology to provide direct input/output interface with TTL and DTL logic families. All inputs are protected to prevent damage from static charge accumulation.

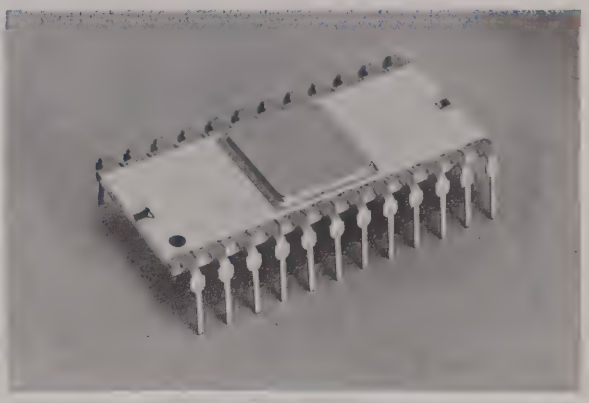
The MK 2302 P is preprogrammed with ASCII-encoded characters (font shown on back page). Other ROMs in the series are programmed during manufacture to customer specifications by modification of a single mask.

Characters are selected by a six-bit binary word at the Character Address inputs. Each character consists of five columns, the columns selected by an internal counter which is clocked by the Counter Clock input. Column information appears sequentially beginning with the left-most column. Two additional intercharacter spacing columns are available, selectable for one or two spaces by the Count Control Input. During spacing, the Data Outputs are high (+5V), or the "dot-off" condition. After the last space, the modulo counter automatically increments to the leftmost column.

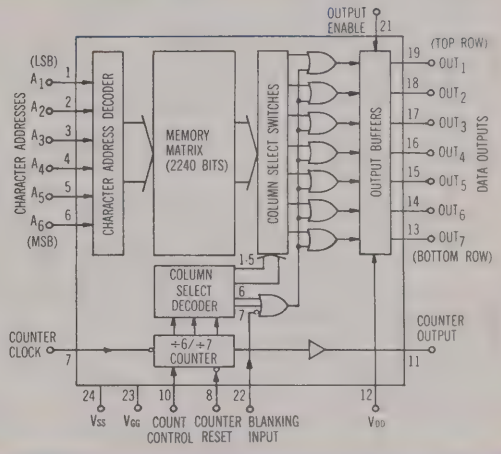
Synchronizing other system components with the ROM is possible using the Counter Reset Input to reset the counter to the last intercharacter spacing column, or using the Counter Output which occurs only on the last spacing column.

The Blanking Input allows all Data Outputs to be driven high (+5V) without affecting any other ROM functions. The Output Enable input allows the outputs to be open-circuited for wire-ORing.

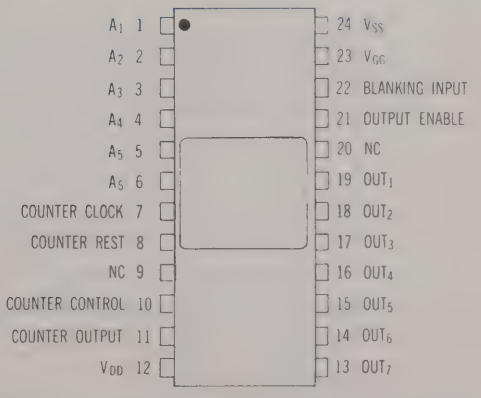
Memory operation is static; refresh clocks are not required to maintain output information. The Counter Clock input is used only to select columns and need not be pulsed continuously.



FUNCTIONAL DIAGRAM



PIN CONNECTIONS



NC = NO CONNECTION

MOSTEK

absolute maximum ratings

Voltage on any terminal relative to V_{SS} ..... +0.3V to −20V
Operating temperature range ..... 0°C to +75°C
Storage temperature range ..... −55°C to +150°C

recommended operating conditions ($0°C \leq T_A \leq 75°C$)

	PARAMETER		MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage	+4.75	+5.0	+5.25	V	
	V_{DD}	Supply voltage	—	0.0	—	V	See note 1
	V_{GG}	Supply voltage	−12.6	−12.0	−11.4	V	
INPUTS	$V_{in(o)}$	Input voltage, logic "0"			+0.6	V	See note 2
	$V_{in(I)}$	Input voltage, logic "I"	$V_{SS}-1.5$			V	Count control input should be
	$V_{in(cc)}$	Count Control input voltage, ÷6		−12.0	−11.4	V	returned to V_{GG} for ÷6 oper-
		÷7	+4.75	+5.0		V	ation, or V_{SS} for ÷7 operation
COUNTER TIMING	f_{clk}	Counter Clock input frequency	0		200	kHz	
	$t_{clk(o)}$	Clock time at logic "0"	2			μs	
	$t_{clk(I)}$	Clock time at logic "I"	2			μs	See timing diagrams
	$t_{r(clk)}$	Clock rise time			0.1	μs	
	$t_{f(clk)}$	Clock fall time			0.1	μs	
	t_{rp}	Reset pulse width	1.0			μs	
	t_{crd}	Clock-to-reset pulse delay	0.4			μs	See note 4

electrical characteristics (V_{SS} = +5.0V ±0.25V, V_{GG} = −12.0V ±0.6V, 0°C ≤ T_A ≤ +75°C, unless noted otherwise)

	PARAMETER		MIN	TYP*	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Supply current (V_{SS})		20	40	mA	Outputs unconnected
	I_{GG}	Supply current (V_{GG})		20	40	mA	f_{clk} = 200 kHz
INPUTS	C_{in}	Input capacitance			10	pF	$V_{in}=V_{SS}$, f_{meas} = 1MHz
	I_{in}	Input leakage current			10	μA	$V_{in}=V_{SS}-6V$, T_A = 25°C
OUTPUTS	$V_{out(o)}$	Output voltage, logical "0"		0.2	0.4	V	I_{out} = 2.0 mA (into output)
	$V_{out(I)}$	Output voltage, logical "I"	2.4			V	I_{out} = 0.6 mA (out of output)
	I_{out}	Data Output leakage current	−10		+10	μA	$V_{SS}-6V \leq V_{out} \leq V_{SS}$, T_A = 25°C (outputs disabled)
DYNAMIC CHARACTERISTICS	t_{AO}	Address-to-output delay time			1	μs	
	t_{CO}	Clock-to-output delay time			1	μs	
	t_{CCO}	Clock-to-counter output delay time			1	μs	Rise and fall times included in delay times
	t_{BO}	Blanking/unblanking delay time			1	μs	
	t_{OEO}	Output enable/disable delay time			1	μs	
	t_{CRO}	Counter reset delay time			1	μs	R_L = 4 kΩ to V_{SS}
	t_{CRCO}	Reset-to-counter output delay time			1	μs	C_L = 15 pF to V_{DD}
	t_F	Output fall time			0.3	μs	T_A = 25°C
	t_R	Output rise time			0.3	μs	

See note 1 (POWER); See note 2 (INPUTS); See timing diagrams (COUNTER TIMING); See note 4 (COUNTER TIMING); See note 2 (INPUTS); See note 3 (OUTPUTS); See timing diagrams (DYNAMIC CHARACTERISTICS)

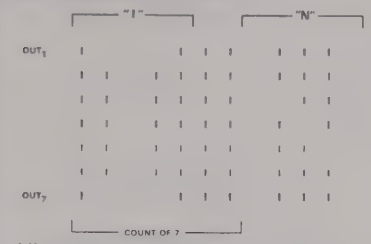
*Typical values apply at V_{SS} = +5.0V, V_{GG} = −12.0V, T_A = 25°C

NOTES:
1. Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., V_{SS} = 0V, V_{DD} = −5V, V_{GG} −17V. Input voltages would also need to be adjusted accordingly.
2. These parameters apply to the character address, counter clock, counter reset, blanking, and output enable inputs.
3. These parameters apply to both the data outputs and counter output.
4. The counter clock must not make a negative transition within the period tcrd, before or after a positive counter reset transition. The counter reset negative edge may occur any time.

timing

(waveforms not to scale)

Timing diagram (1) shows the time relationships between character address, data output, counter clock, and counter output during typical operation of an MK 2300 P Series character generator. An output sequence from the MK 2302 P is shown to help clarify operation. This sequence can be seen from the top rows (OUT_1) of the characters "I" and "N".



All timing relationships shown in diagram (1) apply to any other output or combination of characters as well.

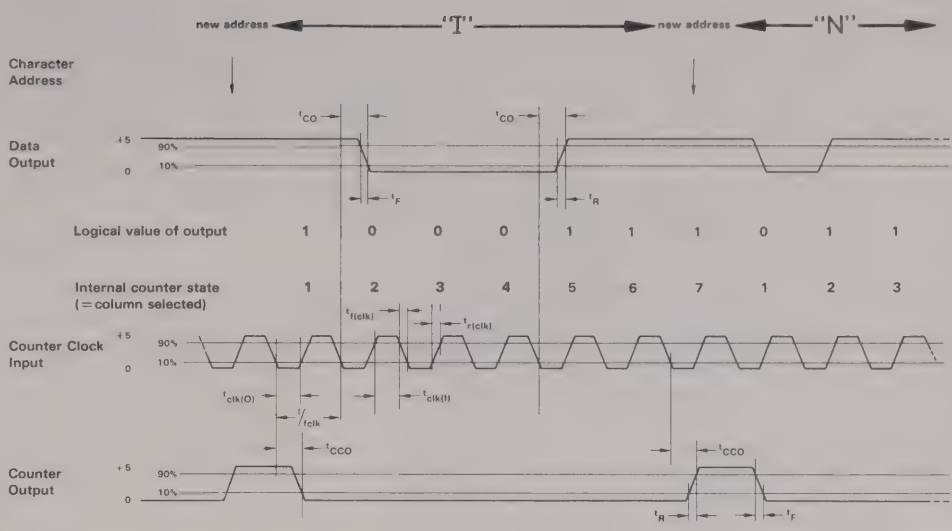
Relevant input conditions assumed but not shown in timing diagram (1) are as follows:

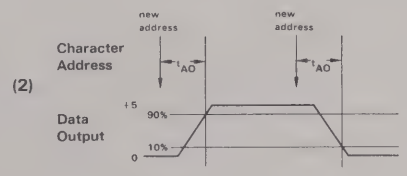
Count Control,	+5V
Counter Reset,	+5V
Blanking Input,	+5V
Output Enable,	+5V

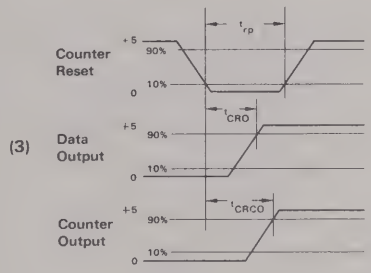
Had the Count Control input been at −12V, the counter sequence would have been six positions instead of seven and the Counter Output would have been high during the sixth position.

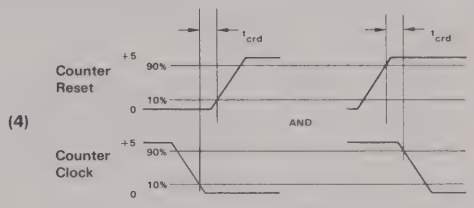
New character addresses are shown coinciding with the rising edge of the Counter Output waveform in diagram (1). This condition was selected to demonstrate use of the Counter Output to advance an external input register to a new character address. Character addresses can be changed at any other time as well. Timing diagram (2) depicts output response to a character address change when, for example, the counter is stationary in one of the five character column positions.

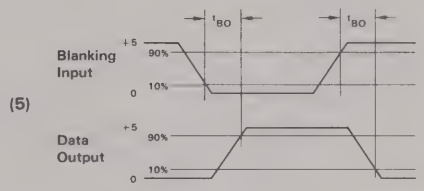
Timing diagrams (3) through (6) show timing relationships for the Counter Reset, Blanking Input, and Output Enable. The "open" condition in (6) implies that both the pull-up and pull-down devices in each data output push-pull buffer are turned off.

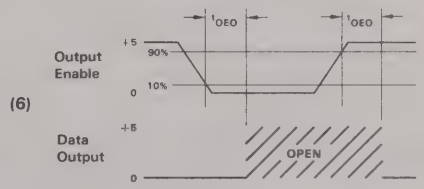












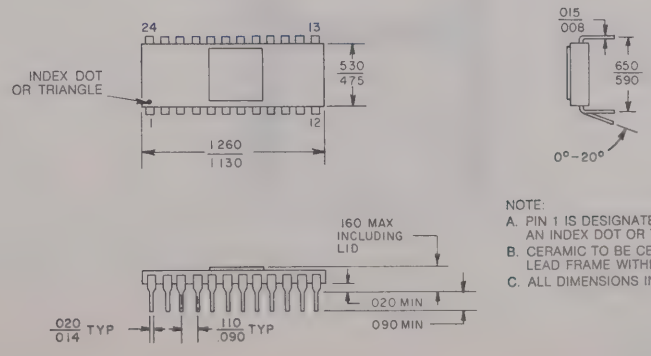
operating notes

The following table summarizes the MK 2300 P Series input control states and corresponding drive levels:

Count Control	
÷6	−12V
÷7	+5V
Counter Reset	
operate	+5V
reset	0V
Blanking Input	
unblank	+5V
blank*	0V
Output Enable	
enable	+5V
disable**	0V

*All data outputs high (+5V)
**All data outputs open-circuited

physical description (24 lead ceramic dual-in-line hermetic package)



NOTE:
A. PIN 1 IS DESIGNATED BY AN INDEX DOT OR TRIANGLE
B. CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN .020"
C. ALL DIMENSIONS IN INCHES

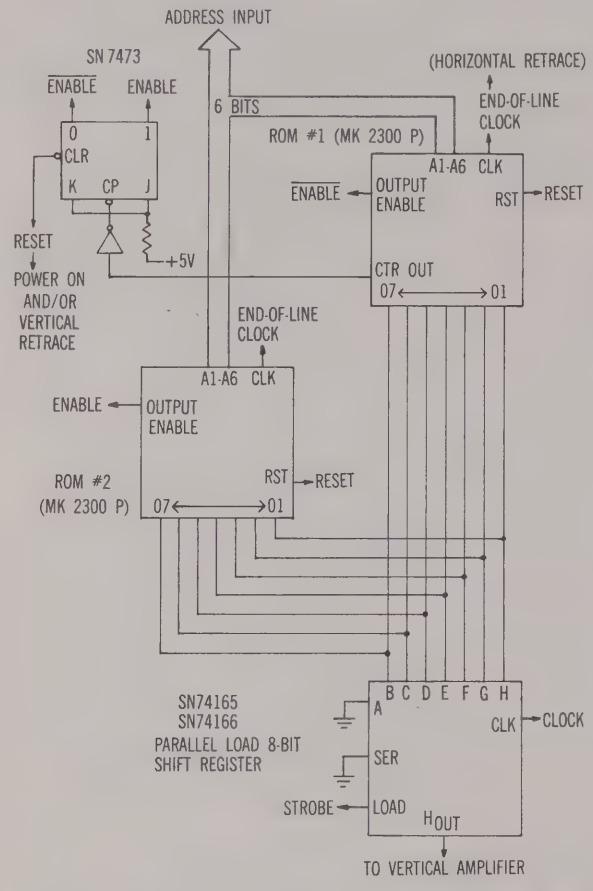
2240 BIT MOS Read-Only Memory Character Generators

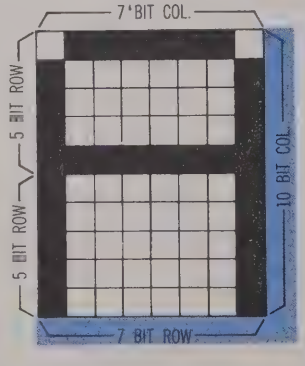
APPLICATION: 7x10 CHARACTER GENERATOR

ROM CODING

7x10 Non-Interlace Configuration: (As illustrated) For row-out (7-bit) horizontal raster-scan application, code ROM #1 for Rows 1 through 5; and ROM #2 for Rows 6 through 10.

7x10 Interlace (525-line): Code ROM #1 for Rows 1, 3, 5, 7, 9; Code ROM #2 for Rows 2, 4, 6, 8, 10. The Enable Flip-flop should be changed to clock only at vertical retrace time, thus allowing ROM #1 to be enabled for the 1st page sweep (262 ½ lines) and then allowing ROM #2 to be enabled for the interlaced 2nd page sweep of 262 ½ lines.



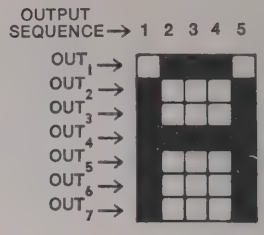


Combining two 5x7 column-output ROMs provides a 7x10 row output.

MK 2302 P

Logic 1 = input @ +5V
Logic 0 = input @ 0V

Output dot "on" = 0V
Output dot "off" = +5V



A_4	A_3	A_2	A_1	A_6 1 1 0 0 / A_5 0 1 0 1
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

DS-24001270-3 JULY 1972

2560 BITS (256x10)

MOS Read Only Memory

MOSTEK

FEATURES

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Chip enable permits wire-ORing
- ☐ Custom-programmed memory requires single mask modification
- ☐ 550 ns cycle time ($0° \leq T_A \leq 75°C$)
- ☐ Static output storage latches
- ☐ Optional 3-bit, chip-select decoder available
- ☐ 2560 bits of storage, organized as 256 10-bit words
- ☐ Operates from +5V and −12V supplies

APPLICATIONS

- ☐ Look-up table
- ☐ Code converter
- ☐ Stroke character generator
- ☐ Dot-matrix character generator

DESCRIPTION

The MK 2400 P Series TTL/DTL-compatible MOS Read-Only Memories (ROM's) are designed for a wide range of general-purpose memory applications where large quantity bit storage is required. Each ROM provides 2560 bits of programmable storage, organized as 256 words of 10 bits each. Low threshold-voltage processing, utilizing ion implantation with P-channel enhancement-mode MOS technology, provides direct input/output interface with TTL and DTL logic.

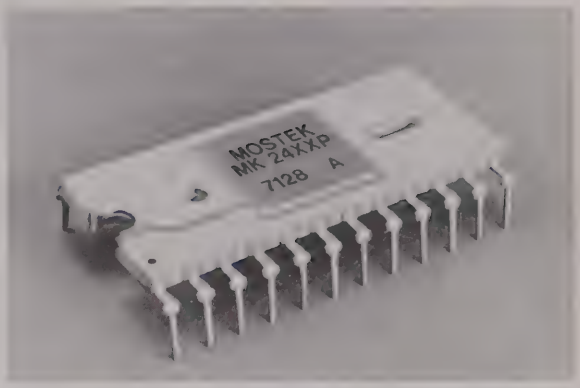
Programming is accomplished during manufacture by modification of a single mask, according to customer specifications. The MK 2400 P Series is available in either 24-lead or 28-lead ceramic dual-in-line packages. On the 28-pin ROM, an optional Chip Select Decoder may also be programmed according to customer specifications to provide a 3-bit Chip Select Code.

Operation involves transferring addressed information from the memory matrix into the storage latches using the READ and $\overline{\text{READ}}$ inputs (see Timing). Information stored in the latches will remain despite address changes or chip disabling until the READ and $\overline{\text{READ}}$ inputs are again cycled. READ and $\overline{\text{READ}}$ input signals may be generated from separate timing circuits if desired, or either may be the inverse of the other.

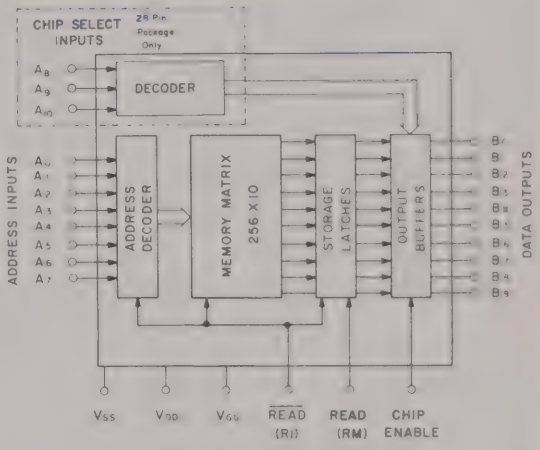
The Chip Enable input forces the normally push-pull output buffer stages to an open-circuit condition when disabling the chip. If desired, new data can be stored in the storage latches while the chip is disabled. When the chip is re-enabled, this data would be present at the outputs.

All inputs are protected against static charge accumulation. Pull-up resistors on all inputs are available as a programmable option.

For additional information regarding custom programming and coding sheets, contact your nearest Mostek representative.



FUNCTIONAL DIAGRAM



OPERATING NOTES

CHIP ENABLE	READ	$\overline{\text{READ}}$	OUTPUT
0	X	X	A
1	0	1	B
1	1	0	C

"1" = V_{SS} (+5V); "0" = V_{DD} (0V)

X = No effect on output

A = Output open-circuited

B = Output retains data last stored in latches

C = Output assumes state of addressed cells

1215 W. Crosby Road, Carrollton, Texas 75006

MOSTEK®

absolute maximum ratings

Voltage on any terminal relative to V_{SS} ..... +0.3V to −20V
Operating temperature range ..... 0°C to +75°C
Storage temperature range ..... −55°C to +150°C

recommended operating conditions ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage	+4.75	+5.0	+5.25	V	See note 1
	V_{DD}	Supply voltage	—	0.0	—	V	
	V_{GG}	Supply voltage	−12.6	−12.0	−11.4	V	
INPUTS	$V_{in(o)}$	Input voltage, logic "0"		0	+0.8	V	Pull-up resistors (≈5KΩ) to V_{SS} available as programmable option.
	$V_{in(l)}$	Input voltage, logic "1"	$V_{SS}-1.5$	V_{SS}		V	
INPUT TIMING	t_{cyc}	Address change cycle time	550			ns	
	t_{ld}	Address to $\overline{\text{Read}}$ lead time	250			ns	
	t_{lg}	Read lag time	−1.0		.05	μs	See Timing Section
	$t_{\overline{rd}}$	$\overline{\text{Read}}$ pulse width	300			ns	
	t_{rd}	Read pulse width	0.3		100	μs	
	t_r	Rise time, any input			100	ns	
	t_f	Fall time, any input			100	ns	

electrical characteristics (V_{SS} = +5.0V ±0.25V, V_{GG} = −12.0V ±0.6V, 0°C ≤ T_A ≤ +75°C, unless noted otherwise. Pull-up resistors not programmed.)

		PARAMETER	MIN	TYP*	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Supply current (V_{SS})		12	25	mA	Outputs unconnected
	I_{GG}	Supply current (V_{GG})		−12	−25	mA	See Note 2 and Note 3
INPUTS	C_{in}	Input capacitance		5	10	pF	$V_{in}=V_{SS}$, f_{meas} = 1MHz
	I_{in}	Input leakage current			10	μA	$V_{in}=V_{SS}$ −6V T_A = 25°C
OUTPUTS	$V_{out(o)}$	Output voltage, logical "0"			0.4	V	I_{out} = 1.6 mA (into output)
	$V_{out(l)}$	Output voltage, logical "1"	2.4			V	I_{out} = 0.4 mA (out of output)
							$V_{SS}-6V \leq V_{out} \leq V_{SS}$
	I_{out}	Output leakage current	−10		+10	μA	T_A = 25°C (outputs disabled)
DYNAMIC CHARACTERISTICS	t_{ACC}	Address-to-output access time			600	ns	t_{ld} = 250ns, t_{lg} = 0ns
	t_{OD}	Output delay time			350	ns	
	t_{OEO}	Output enable/disable time		125	300	ns	

See note 3 and Figure #1

See timing Section and Figure #1

*Typical values apply at V_{SS} = +5.0V, V_{GG} = −12.0V, T_A = 25°C

NOTES:
1. Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., V_{SS} = 0V, V_{DD} = −5V, V_{GG} = −17V. Input voltages would also need to be adjusted accordingly.
2. Max measurements at 0°C. (MOS supply currents increase as temperature decreases.) I_{SS} will increase 1.6mA (max) for each input at logic 0 when pull-up resistors are programmed.
3. Unit operated at minimum specified cycle time.

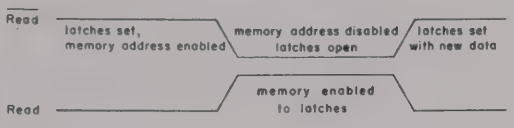
timing

(waveforms not to scale)

Notes:

1. All times are referenced to the 1.5V point relative to V_{DD} (ground) except rise and fall time measurements.
2. Chip enable = V_{SS} for all measurements except when measuring T_{OEO}.
3. Logic 0 is defined as V_{DD} or ground; logic 1 as V_{SS} or +5V.

INTERNAL FUNCTION OF READ/ READ SIGNALS



Set up time, t_{id}, allows the input address to propagate through the address decoder and memory matrix prior to $\overline{READ}$ logic 0 time. As indicated above, $\overline{READ}$ at a logic 0 internally disables the input address so that an external address change may occur without affecting the location previously selected. The latches are also readied to receive new data which is enabled from the matrix when READ is at a logic 1. Data is set in the latches when $\overline{READ}$ is allowed to rise back to its logic 1 state. In actual use, the READ rising and falling edges can preceed the falling and rising edges of $\overline{READ}$, respectively, as implied by the specification of negative lag times, t_{ig}. This allows a very flexible timing relation between the two pulses, in that either input can be the inversion of the other or both may be generated from separate timing circuits.

Output data appears following the rise of the READ pulse but correct output data will not appear until $\overline{READ}$ has gone low. For this reason, $\overline{READ}$ is shown preceding READ even though other relationships are allowed. If READ is made to precede READ, delay time, t_{OD}, should be referenced to the fall of $\overline{READ}$ rather than as shown.

The chip is disabled by applying a logical 0 to the chip enable input, forcing the outputs to an open-circuit condition. The output data present at the time of disable will again be present upon re-enabling unless a new read cycle was initiated for a different address while the chip was disabled, in which case the new data would be present at the outputs.

The programmable 3-bit chip select timing would be the same as the address inputs.

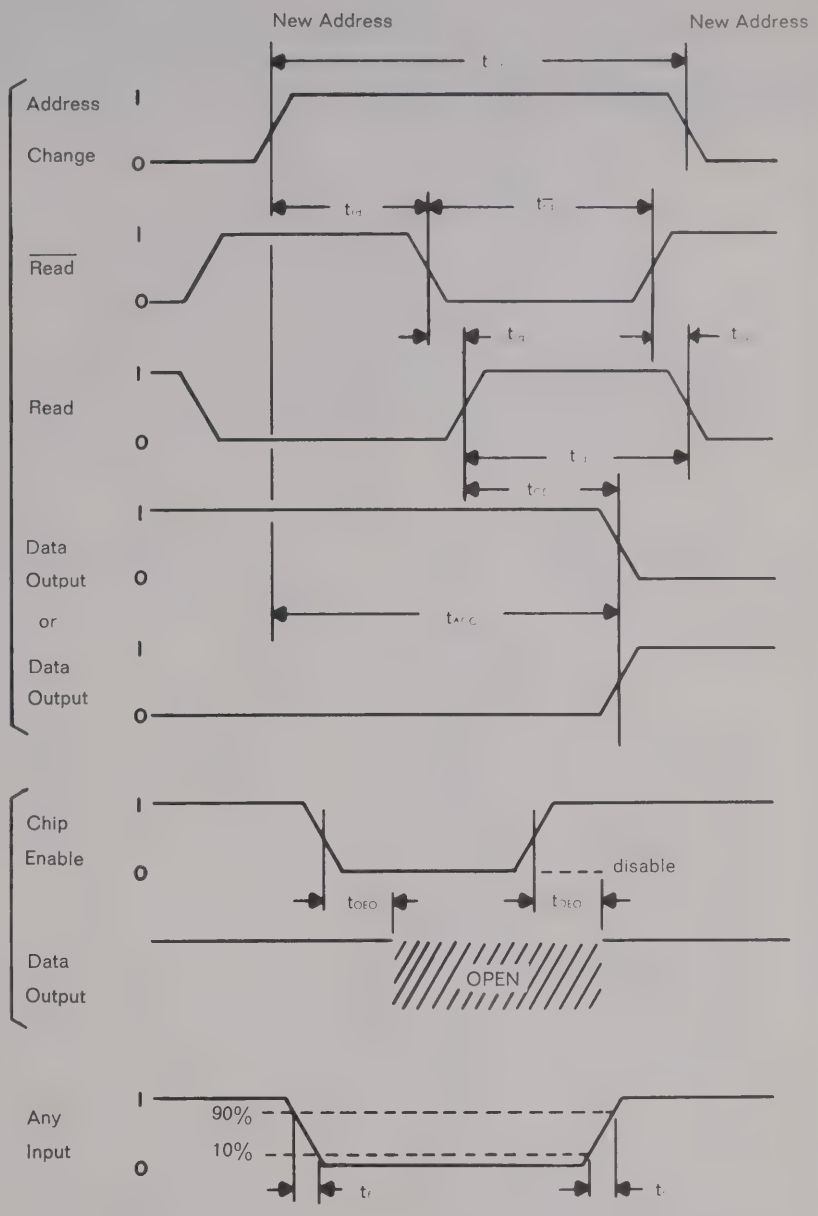
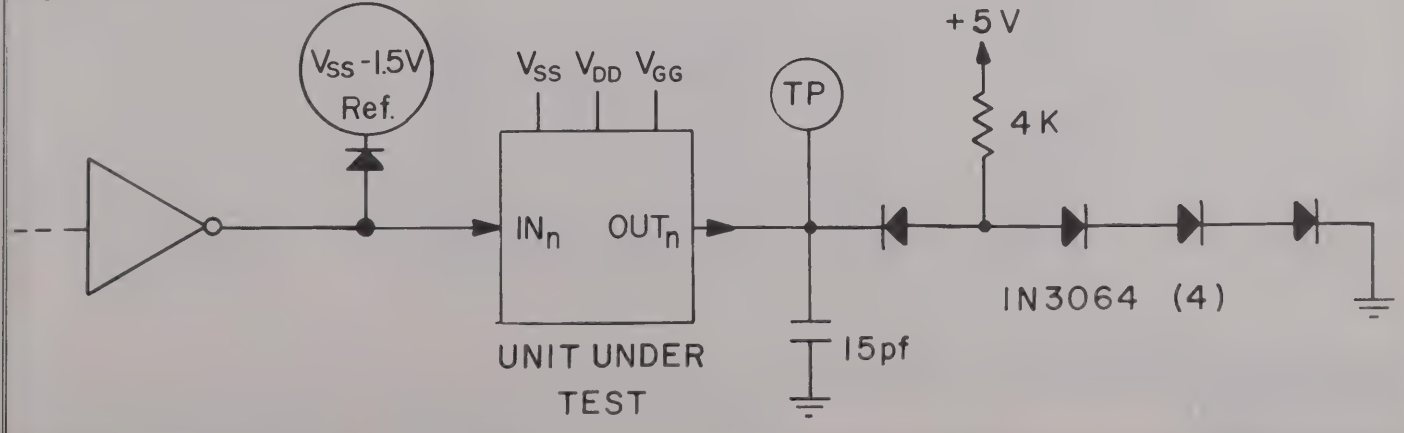
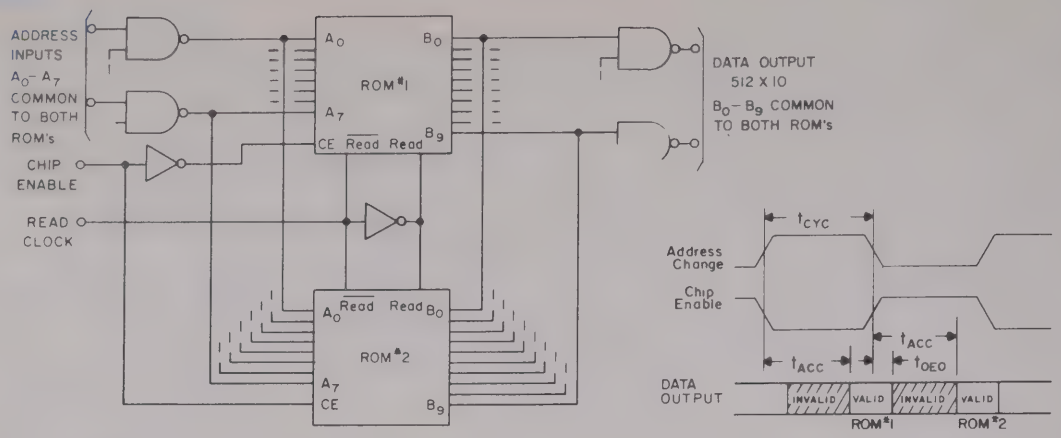


figure #1 (Test Circuit)



MK 2400 P SERIES MOS ROM

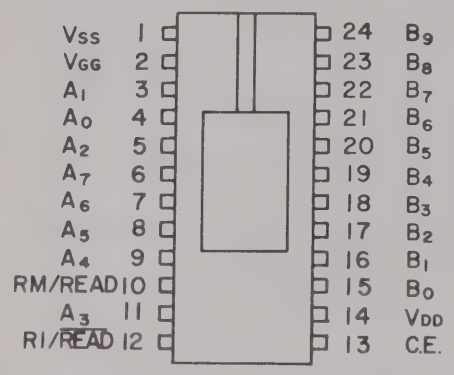
APPLICATIONS



Application shows wire-Or'ing for expansion to a 512 X 10 memory. Further expansion is possible by 1 of N decoding to the Chip Enable input (or with the optional 3-bit decoder) while maintaining the time relationships shown. t_{cyc} should include the desired data-valid time. Interface devices may be TTL or DTL.

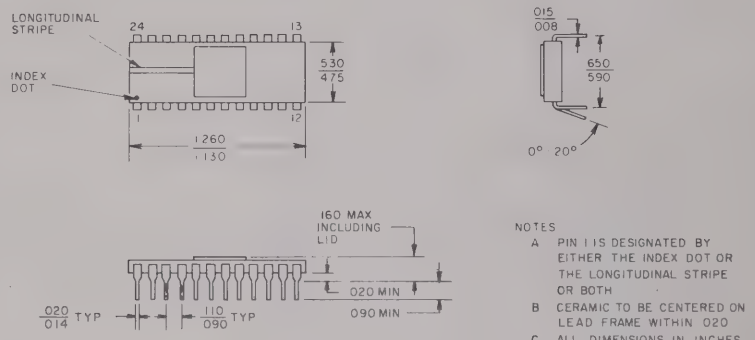
PIN CONNECTIONS

top view, 24 pin CDIP



PHYSICAL DESCRIPTION

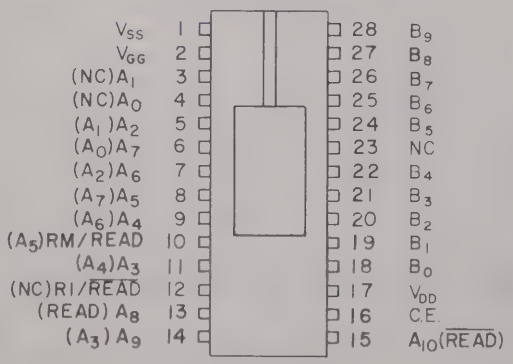
(24 lead ceramic dual-in-line hermetic package)



NOTES
- A PIN 1 IS DESIGNATED BY EITHER THE INDEX DOT OR THE LONGITUDINAL STRIPE OR BOTH
- B CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN 020
- C ALL DIMENSIONS IN INCHES

PIN CONNECTIONS

top view, 28 pin CDIP

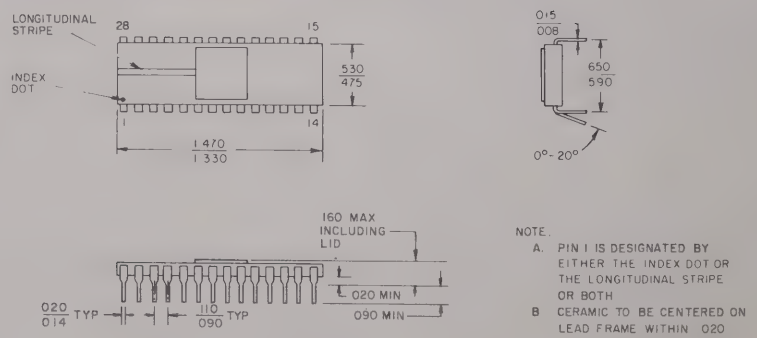


N.C. = no connection

( ) OPTIONAL PIN ARRANGEMENT

PHYSICAL DESCRIPTION

(28 lead ceramic dual-in-line hermetic package)



NOTE
- A. PIN 1 IS DESIGNATED BY EITHER THE INDEX DOT OR THE LONGITUDINAL STRIPE OR BOTH
- B CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN 020
- C ALL DIMENSIONS IN INCHES

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MK 2408 P

DS-24001270-1/DEC. 1970

2560 BIT
MOS Read-Only Memory Character Generator

MOSTEK

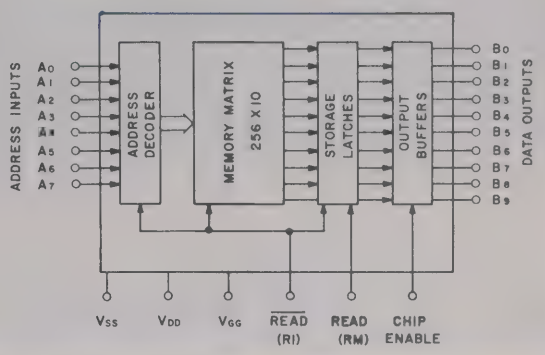
DESCRIPTION

The MK 2408 P is a pre-programmed member of the MK 2400 P Series. It is programmed as a dot-matrix character generator (64 characters) with ASCII encoded inputs and row (5-bit) outputs. The MK 2408 P outputs two rows at the same time. Row 1 is available at outputs B9 (left), B8, B7, B6, and B5 (right) while row 2 is available at outputs B4 (left), B3, B2, B1, and B0 (right). Row 3 is available at B9 through B5 while row 4 is available at B4 through B0. Row 5 and row 6 are available at B9 through B5 and B4 through B0. Row 5 and row 6 are available at B9 through B5 and B4 through B0. Row selection is determined by the address combination of bits A0 and A1.

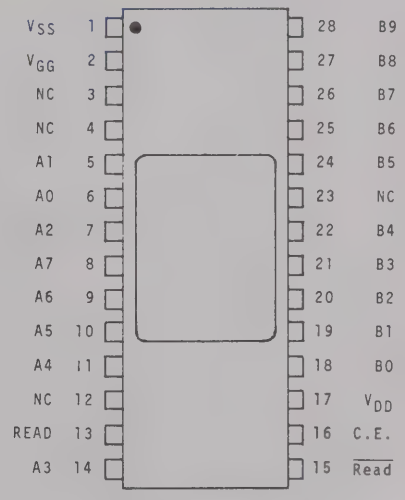
The MK 2408 P meets and operates by the specifications outlined in the MK 2400 P Series data sheet (DS-24001270-2)

The example in Figure 1 demonstrates the correspondence of the device outputs and row select sequence to the 7 X 5 dot-matrix font. The complete character font patterns (truth table) are illustrated on the back. A logic 1 or a DOT represents an input or output voltage equal to V_{SS} (+5V) and a logic 0 or a blank represents a voltage equal to V_{DD} (0V). The eighth row outputs (B4 through B0 when inputs A1 and A0 equal logic 1) are not illustrated since in each case they are equal to all 0's.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



NC= NO CONNECTION

A1	A0		B9 B4	B8 B3	B7 B2	B6 B1	B5 B0		
0	0	—	1	0	0	0	1	--	B9-B5
		—	1	1	0	1	1	--	B4-B0
0	1	—	1	0	1	0	1	--	B9-B5
		—	1	0	1	0	1	--	B4-B0
1	0	—	1	0	0	0	1	--	B9-B5
		—	1	0	0	0	1	--	B4-B0
1	1	—	1	0	0	0	1	--	B9-B5
		—	0	0	0	0	0	--	B4-B0

A7 = 0
A6 = 0
A5 = 1

A4 = 1
A3 = 0
A2 = 1

FIGURE 1

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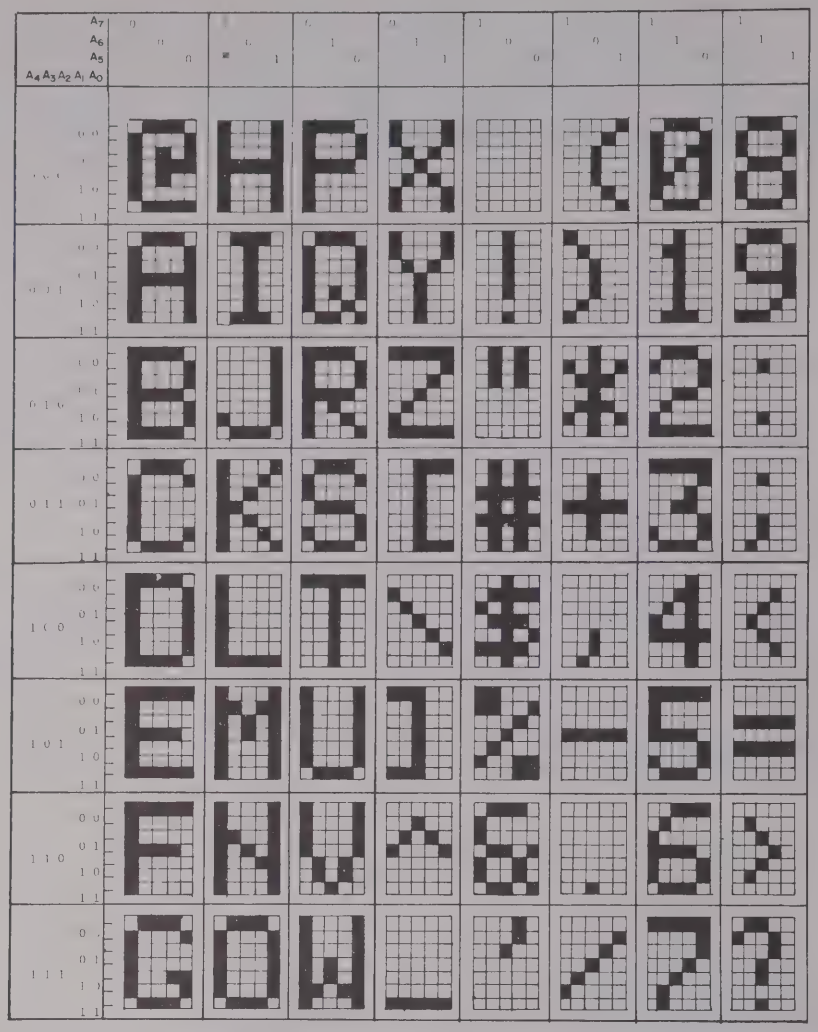
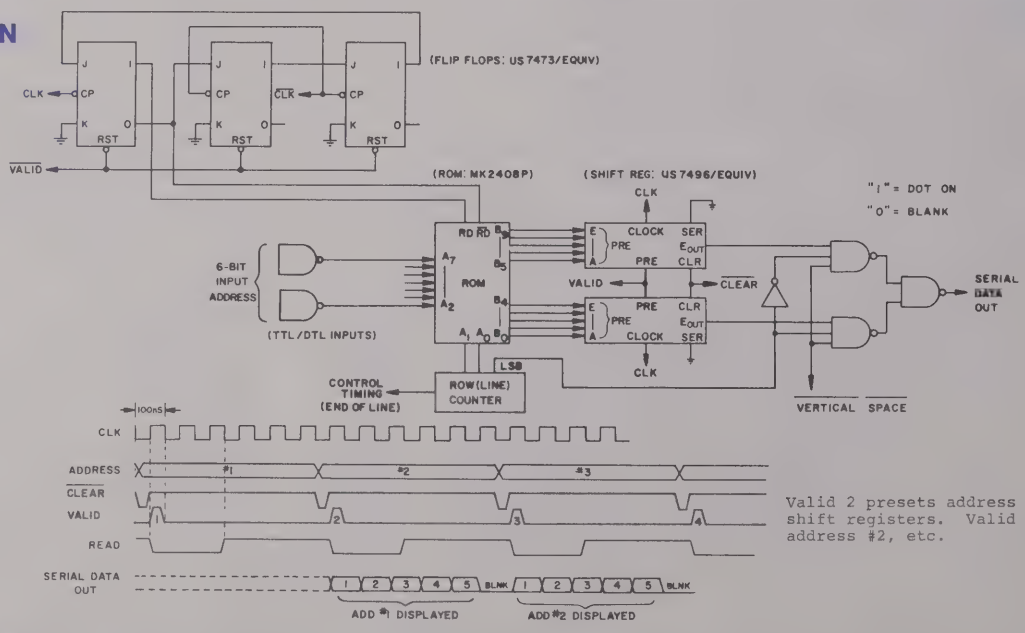
MOSTEK®

CODING & CHARACTER FONTS



APPLICATION



Valid 2 presets address #1 data in shift registers. Valid 3 presets address #2, etc.

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MOS Random Access Memories

4000 - 4999

PRODUCTS

APPLICATIONS NOTES

MISCELLANEOUS

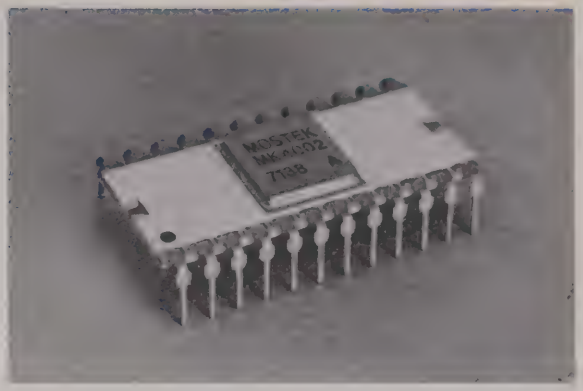
MOSTEK CORPORATION

MK 4002 P

DS-40021170-2/OCT. 1971

256-BIT (64 x 4)
MOS Random Access Memory

MOSTEK



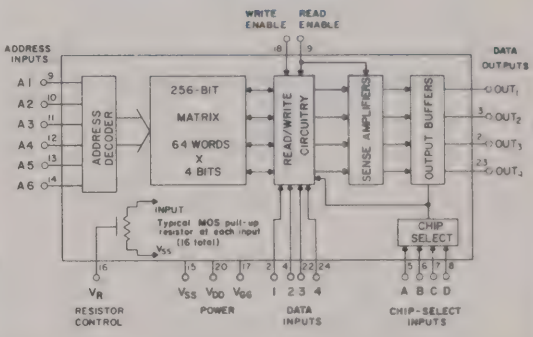
FEATURES

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Full on-chip address decoding
- ☐ Access and cycle times under 1 μs
- ☐ Low power dissipation: typically under 200 mW
- ☐ Convenient organization; 64 words × 4 bits
- ☐ Static operation
- ☐ Chip-select inputs for memory expansion
- ☐ Operates from +5V and −12V supplies

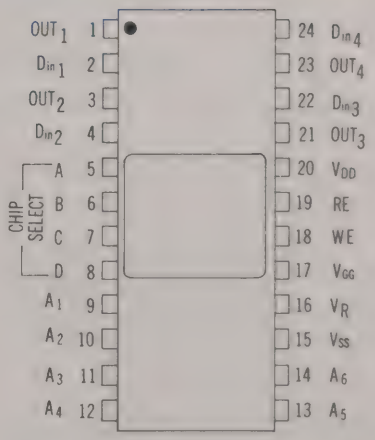
APPLICATIONS

- ☐ Scratchpad memories
- ☐ Data link buffers
- ☐ Key-to-tape buffers
- ☐ Tape-to-printer buffers
- ☐ Editing memories

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



DESCRIPTION

The MK 4002 P is a 256-bit, MOS read/write, random-access memory (RAM), organized as 64 words of 4 bits each. Address decoding is performed internally from binary address; external decoders are not required. Read/write control logic, sense circuitry, and output buffers (each capable of directly driving one TTL load) are also included. Memory contents are read out non-destructively (NDRO).

Low-threshold voltage processing utilizing ion-implantation is employed with P-channel enhancement-mode MOS technology to provide direct input/output interface with TTL and DTL logic families. All inputs are internally protected to prevent damage due to static charge accumulation.

All logic inputs can be driven directly from TTL or DTL. A pull-up resistor is internally provided at each input for use when driving from TTL. A separate control input (V_R, pin 16) allows these resistors to be disabled when not required. Memory operation is static; refresh clocks are not necessary to maintain stored data in the memory. Separate read and write enable inputs are provided to facilitate synchronous data transfer. Memory outputs can be wire-ORed to allow system expansion. Outputs can be disabled (open-circuited) by use of the Chip-Select inputs. Four Chip-Select inputs are provided to allow any one of up to 16 wire-ORed memories to be easily selected.

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MOSTEK ®

absolute maximum ratings

Voltage on any terminal relative to V_{SS} ..... +0.3V to −20V
Operating temperature range ..... 0°C to +75°C
Storage temperature range ..... −55°C to +150°C

recommended operating conditions ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage	+4.75	+5	+5.25	V	
	V_{DD}	Supply voltage		0		V	See note 1
	V_{GG}	Supply voltage	−12.6	−12	−11.4	V	
INPUTS	$V_{in(0)}$	Input voltage, logic 0		0	0.8	V	See note 2
	$V_{in(1)}$	Input voltage, logic 1	$V_{SS}-1$	V_{SS}		V	
INPUT TIMING	t_{RE1}	Read-Enable pulse width	400			ns	Fig 1.1
	t_{RC1}	Read cycle time	850			ns	Fig 1.1, $t_{RE1}=400ns$
	t_{RE2}	Read-Enable pulse width	550			ns	Fig 1.2
	t_{RC2}	Read cycle time	1000			ns	Fig 1.2, $t_{RE2}=550ns$
	t_{WE}	Write-Enable pulse width	400			ns	Fig 2 — $t_{WE}=400ns$
	t_{WC}	Write cycle time	650			ns	Fig 2 — $t_{AW}=150ns$
	t_{AW}	Address-to-write delay	150			ns	Fig 2 — $t_{WA}=100ns$
	t_{WA}	Write-to-address delay	100			ns	Fig 2
	t_{lead}	Data lead time	400			ns	Fig 2

electrical characteristics ($V_{SS}=+5.0V \pm 0.25V$, $V_{GG}=-12.0V \pm 0.6V$, $0°C \leq T_A \leq +75°C$, unless noted otherwise)

		PARAMETER	MIN	TYP*	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Supply current (V_{SS})		12	20	mA	See note 3
	I_{GG}	Supply current (V_{GG})		12	20	mA	V_R (pin 16) $=V_{SS}$ Outputs unloaded
INPUTS	C_{in}	Input capacitance		4	6	pF	$V_{in}=V_{SS}$, $f_{meas}=1MHz$, $T_A=25°C$
	$I_{in(1)}$	Input current, logic 1			1	μA	$V_{in}=V_{SS}$, V_R (pin 16) $=V_{SS}$ or V_{GG}, $T_A=25°C$
	$I_{in(0)}$	Input current, logic 0 resistors disabled			−10	μA	V_R (pin 16) $=V_{SS}$, $T_A=25°C$, $V_{in}=0V$
		resistors enabled	.5	−1.1	−1.6	mA	V_R (pin 16) $=V_{GG}$, See note 2
OUTPUTS	C_{out}	Output capacitance		7	10	pF	$V_{out}=V_{SS}$, $f_{meas}=1MHz$, $T_A=25°C$
	I_{out}	Output leakage current	−10		+10	μA	$V_{out}=2.5V$, pins 5, 6, 7, 8 @ 0V
	$V_{out(0)}$	Output voltage, logic 0		0.3	0.5	V	$I_{out}=-1.6mA$
	$V_{out(1)}$	Output voltage, logic 1	2.6			V	$I_{out}=+1.0mA$
DYNAMIC CHAR.	t_p	Output data delay			450	ns	Fig 1.1, 1.2
	$t_{acc(1)}$	Read access time			850	ns	Fig. 1.1, $t_{RE1}=400ns$
	$t_{acc(2)}$	Read access time			1000	ns	Fig 1.2, $t_{RE2}=550ns$

*Typical values apply at $V_{SS}=+5.0V$, $V_{GG}=-12.0V$, $T_A=25°C$

NOTES:
1. Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., $V_{SS}=0V$, $V_{DD}=-5V$, V_{GG} −17V. Input voltages would also need to be adjusted accordingly.
2. Pull-up resistances to V_{SS} (+5V) are provided internally at all 16 inputs (pins 2, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 18, 19, 22, and 24). These resistances are enabled by connecting V_R (pin 16) to V_{GG} and disabled by connection to V_{SS}.
3. The I_{SS} values shown do not include current drawn by the internal pull-up resistances. When these resistances are enabled, I_{SS} will increase 1.6mA (max) for each input at a logic 0.

read cycle

A read cycle is initiated by bringing the read enable input to a logic 1 with the desired address applied. Data outputs then become invalid until a time, tp, following the end of the read enable pulse. During this invalid time period all data outputs will rise to a logic 1 before assuming correct data states of the addressed memory locations.

Chip selection can be made before an address change (Fig. 1.1) or after (Fig. 1.2). Applications #1 and #2 (back page) show an example of the first and second situations, respectively. Read enable pulse width can be shorter when chip selection occurs before an address change, i.e. t_{RE1} (min) < t_{RE2} (min).

Following chip-selection all data outputs go to a logic 0 if sufficient time exists before a read-enable pulse as shown in Fig. 1.1. A read enable pulse is normally required to restore correct output data following any period in which the chip was unselected, even if the input address remains unchanged.

CHIP SELECT PRECEDES ADDRESSING

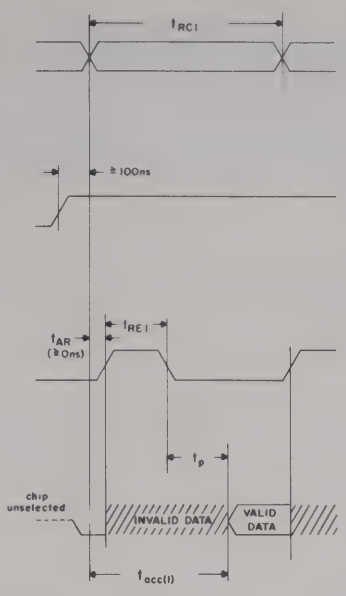


Figure 1.1

CHIP SELECT FOLLOWS ADDRESSING

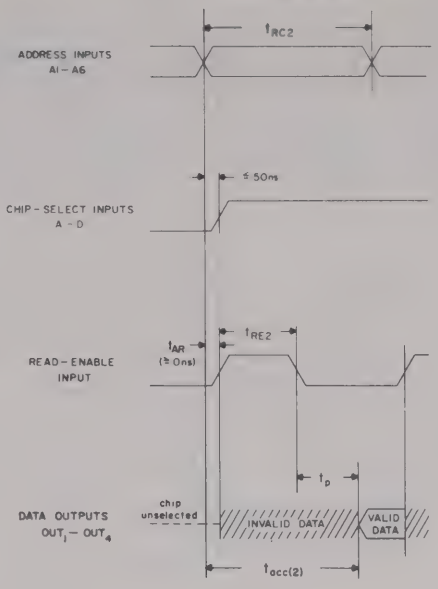


Figure 1.2

write cycle

A write cycle is initiated by bringing the write enable input to a logical 1 with the desired address and data applied. Specified position of the write enable pulse (Fig 2) should be observed to assure correct entry of data into the memory. Data outputs become invalid and fall to a logic 0 following the rise of the write enable pulse, and remain invalid until the next read cycle.

Chip selection can be made before or after an address change without affecting the required width of the write enable pulse.

Writing takes precedence over reading. If both the write enable and read enable inputs are at a logic 1, writing will occur. When a chip is unselected, writing is inhibited and the write enable input cannot affect stored data.

CHIP SELECT PRECEDES OR FOLLOWS ADDRESSING

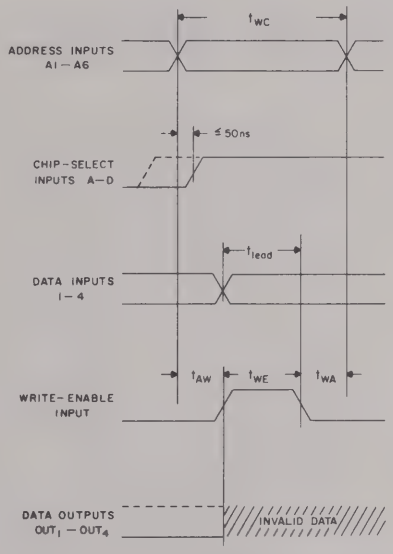
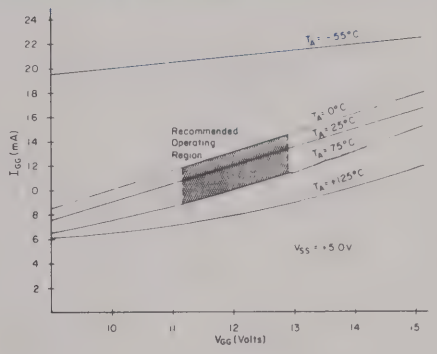
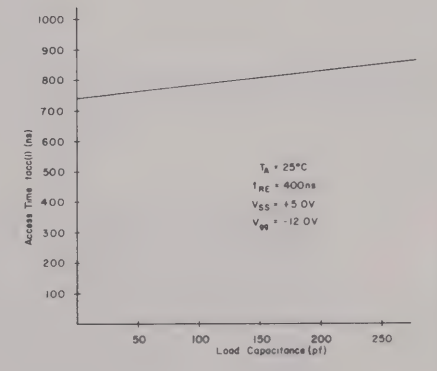
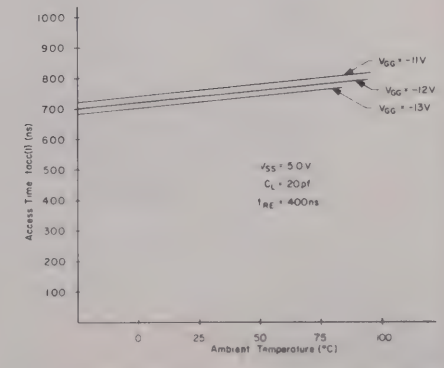


Figure 2

typical performance

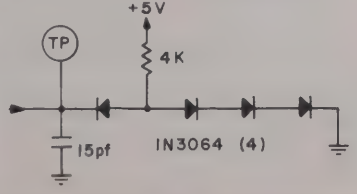






test conditions

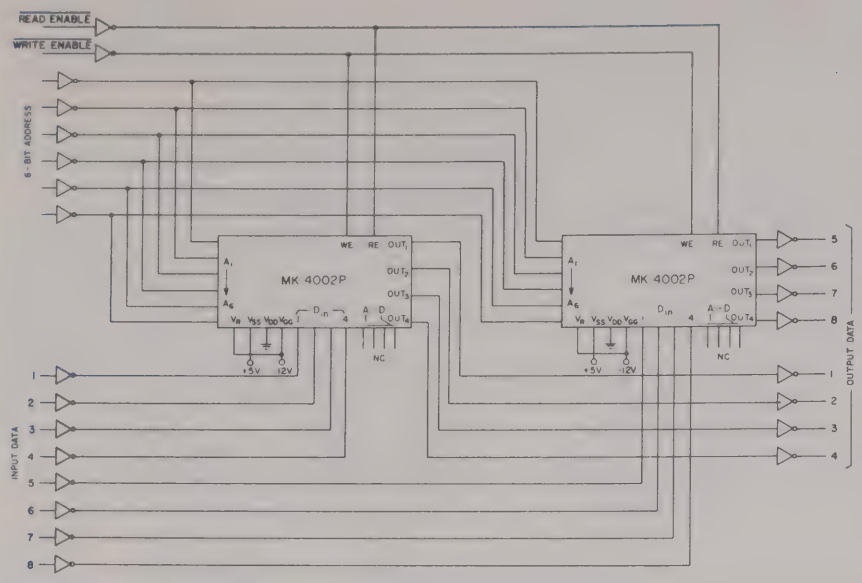
1. All signal swings in Figs. 1.1, 1.2, and Fig. 2 are between V_{DD} (0V) and V_{SS} (+5V).
2. The WE input is at 0V for Figs. 1.1, 1.2. The RE input is at 0V for Fig. 2.
3. All delay measurements are referenced to the +1.5V level. Input pulse rise and fall time is 10ns.
4. Test load (each data output):



operating notes

1. Internal pull-up resistors at the inputs are enabled by connecting V_R, pin 16, to V_{GG} (−12V) and disabled by connection to V_{SS} (+5V).
2. Chip-select inputs A, B, C, and D must all be at a logic 1 for normal operation. If one or more is at a logic 0 the data outputs are open-circuited and writing is inhibited.
3. Unused chip-select inputs should be tied to V_{SS}, but may be left unconnected if the internal pull-up resistors are enabled.
4. A read enable pulse is required following an address change or chip selection in order to achieve specified access and cycle times. However, if either situation occurs without a read enable pulse, the data outputs will become valid given sufficient time, typically 5 μs. This mode can be used where access and cycle time is not an important system parameter.

application (1) 64 words x 8 bits



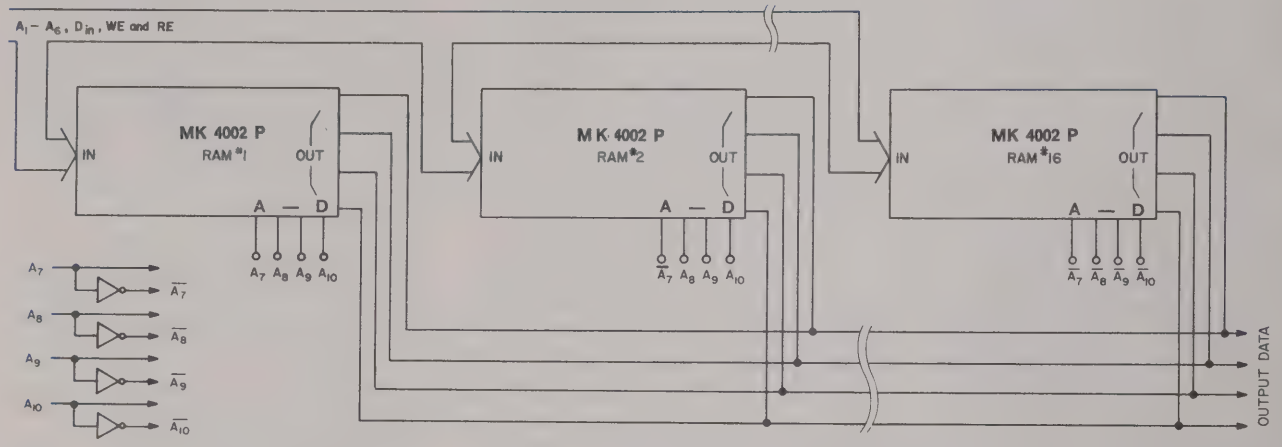
notes:

This application's example shows two MK 4002 P RAMs used in parallel to form a 64 X 8 memory. Address inputs of the two memories are tied in parallel, as are the WE and RE inputs.

Since wire-ORing of the outputs is not necessary for this configuration, the chip-select inputs are not used. Consequently, the shorter of the two read-enable pulse widths, t_{RE1}, can be used and timing Fig. 1.1 is applicable.

The internal input pull-up resistors are enabled ($V_R = V_{GG}$), since the inverters are assumed to be TTL, US 7404 types or equivalents. Other TTL devices with similar input current requirements could be used as well. If DTL logic is used, the internal pull-up resistors can be disabled ($V_R = V_{SS}$) due to the more positive output swing of this logic family. With the internal pull-up resistors disabled, chip-select inputs A-D should be tied to V_{SS} rather than left unconnected.

application (2) 1024 words x 4 bits



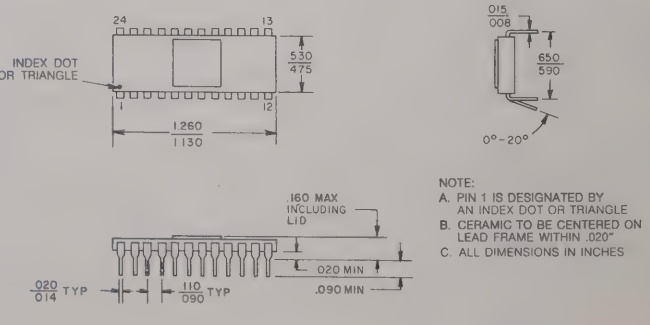
notes:

This applicátion's example demonstrates use of the four chip-select inputs on the MK 4002 P to achieve larger memory sizes by wire-ORing the data outputs. Up to 1024 words of memory can be conveniently achieved in this manner using only four external inverters as shown above. Other electrical connections not shown are similar to those in Application 1. More than 16 packages can be wire-ORed, although additional external circuitry is required.

Because the chip-select inputs are used for addressing in this application, read-enable pulse width t_{RE2} must be used and Fig. 1.2 is applicable for a read cycle. If the faster read cycle, Fig. 1.1, were desired, address inputs A_7 - A_{10} should be applied 100ns prior to the remaining address inputs.

physical description

(24 lead ceramic dual-in-line hermetic package)


INDEX DOT OR TRIANGLE
530 / 475
1.260 / 1130
.015 / .008
.650 / .590
0°-20°
.160 MAX INCLUDING LID
.020 MIN
.090 MIN
.020 / .014 TYP
.110 / .090 TYP
NOTE:
A. PIN 1 IS DESIGNATED BY AN INDEX DOT OR TRIANGLE
B. CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN .020"
C. ALL DIMENSIONS IN INCHES

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MK 4006 P • MK 4006-6 P
MK 4008 P • MK 4008-6 P

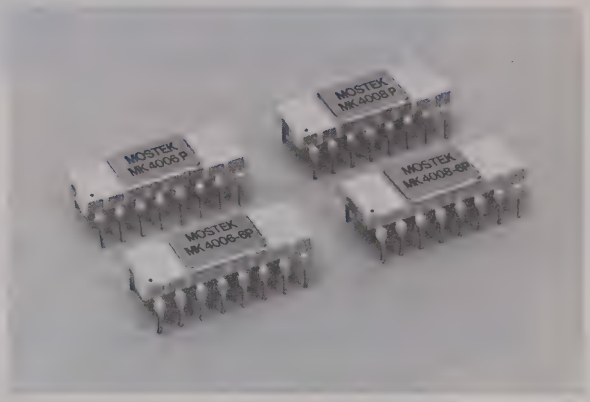
DS-4006572-2/AUG. 1972

1024x 1 BIT DYNAMIC
MOS Random Access Memory

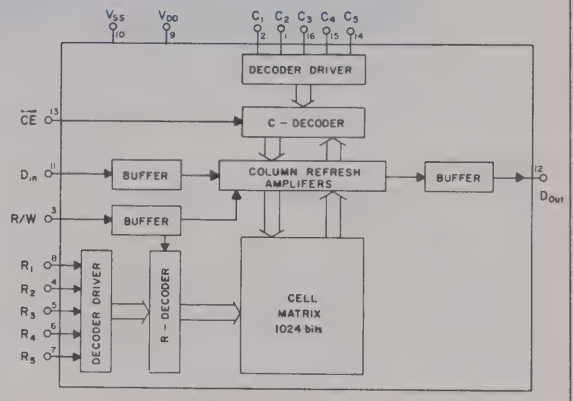
MOSTEK CORPORATION

FEATURES:

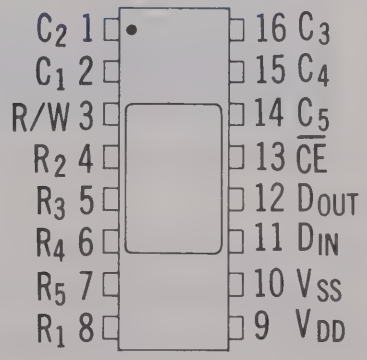
- ☐ TTL/DTL compatible inputs
- ☐ No clocks required
- ☐ Access time:
  MK 4006, −6 P: under 400 ns
  MK 4008, −6 P: under 500 ns
- ☐ Standby power: under 50 mW
- ☐ 16-pin standard CDIP
- ☐ Supply voltage: +5V and −12V



FUNCTIONAL DIAGRAM



PIN CONNECTIONS



DESCRIPTION

This is a family of MOS dynamic 1024x1 random-access memories having identical functional characteristics, differing only in speed and power-down capabilities. Access time in the MK 4006 P is less than 400 ns; in the MK 4008 P, less than 500 ns. The MK 4006-P and the MK 4008-6 P are identical to the MK 4006 P and MK 4008 P, respectively, except that they are specially tested for power down operation.

Full address decoding is provided internally. Information is read out non-destructively (NDRO) and has the same polarity as the input data.

TTL/DTL compatibility at all inputs allows economical use in small systems by eliminating the need for special interface circuitry. Large main-memory applications also benefit from the low drive-voltage swings as well as the packing density afforded by the standard 16-pin dual-in-line packaging and low standby power.

The internal memory element of this RAM is a capacitance, and refreshing must be periodically initiated (see TIMING). However, all internal decoding and sensing is static, so that precharging or clocking normally associated with dynamic memories is not required. From the user's viewpoint, memory control and addressing are essentially those of a static device.

Noise suppression measures normally employed in DTL or TTL systems are sufficient. High voltage input swings and high peak-current line drivers are unnecessary for driving memory inputs, and the memory itself does not exhibit large supply current transients.

Data output is single-ended to minimize propagation delay. Output current is sourced from V_{SS} (+5V), and easily sensed using readily available components. A logic 1 at the output terminal appears as a 5,000 Ohm resistor (MK 4006) to +5V; a logic 0 as an open circuit.

The performance of this RAM is made possible by Mostek's ion-implantation process. In addition to offering low threshold voltages for TTL/DTL compatibility and utilizing conventional P-channel processing, ion-implantation allows both enhancement (normally OFF) and depletion (normally ON) MOS transistors to be fabricated on the same chip. By replacing conventional MOS load resistors with constant-current depletion transistors, operational speeds and functional density are increased.

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MOSTEK CORPORATION ®

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... +0.3 to −20V

Operating Temperature ..... 0°C to +70°C

Storage Temperature Range ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS

(0° C ≤ T_A ≤ 70°C)

	PARAMETER	MK 4006,-6P — MK 4008,-6P MIN	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+4.75	+5.25	V	
V_{DD}	Supply Voltage	−11.4	−12.6	V	
V_{IL}	Input Voltage, Logic 0		+0.8	V	
V_{IH}	Input Voltage, Logic 1	V_{SS}−1	V_{SS}	V	
V_{SB}	Standby Supply Voltage (Fig. 4)	V_{SS}−4	V_{SS}−6	V	Note 1

RECOMMENDED AC OPERATING CONDITIONS[2]

(0° C ≤ T_A ≤ 70°C)

	PARAMETER	MK 4006 P MK 4006-6 P MIN	MAX	MK 4008 P MK 4008-6 P MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time (Fig. 1)	400		500		ns	
t_{WC}	Write Cycle Time (Fig. 2)	650		900		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{WP}	Write Pulse Width (Fig. 2)	250		400		ns ns	t_{AW}=400 ns t_{AW}=500 ns
t_{AW}	Address-to-Write Delay (Fig. 2)	400		500		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{DLD}	Data-to-Write Lead Time (Fig. 2)	300		400		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{RDLY}	Refresh Time (Fig. 3)		2		2	ms	See Note 3.
t_{CDPD}	Chip-Disable-to-Power-Down Delay (Fig. 4)	200		200		ns	See Note 1 See Note 4

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C ≤ T_A ≤ 70°C unless otherwise noted)

	PARAMETER	MK 4006 P MK 4006-6 P MIN	MAX	MK 4008 P MK 4008-6 P MIN	MAX	UNITS	NOTES
I_{SS}, I_{DD}	Supply Current: At T_A=0°C At T_A=70°C		30 24		30 24	mA mA	Output Open
P_{SDBY}	Power Dissipation, Standby		50		50	mW	$V_{SS}-V_{DD}$ = 5V; Note 1
I_{IH}	Input Current, Logic 1. Any Input	−5	+5	−5	+5	μA	$V_I=V_{SS}-1V$
I_{IL}	Input Current, Logic 0, Any Input	−5	+5	−5	+5	μA	V_I=0.8V
I_{OH}	Output Current, Logic 1	1.0		0.8		mA	Note 5
I_{OL}	Output Current, Logic 0		5		5	μA	

TIMING
(Note 2)

CHIP ENABLING (Fig. 5)

The negative-going $\overline{CE}$ enables the chip, and output data becomes valid within t_{CE} time. Return of the $\overline{CE}$ input to logic 1 disables the chip; data out remains for t_{CD} time.

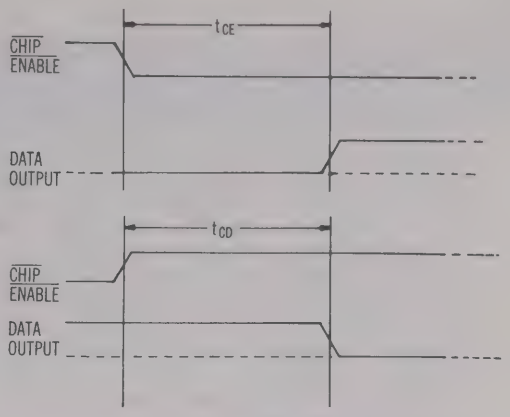


FIG. 5 CHIP ENABLING

TESTING CONSIDERATIONS

For a complete discussion of testing this memory, see Mostek's Applications Note AN-103.

The functional diagram (Fig. 6) indicates signal flow for selected row and column.

A simplified listing of functional tests is shown in Table 1. (high = Logic 1; low = Logic 0)

Tests are performed in an address sequence which requires the maximum number of changes in the row and column decoders between addresses. Addressing Rows 0 through 31 is accomplished by using the binary equivalent of the row address. The internal organization of the memory matrix requires the logic shown in Fig. 7 for column addresses; this logic provides the necessary conversion from binary equivalent to column address.

Fig. 6

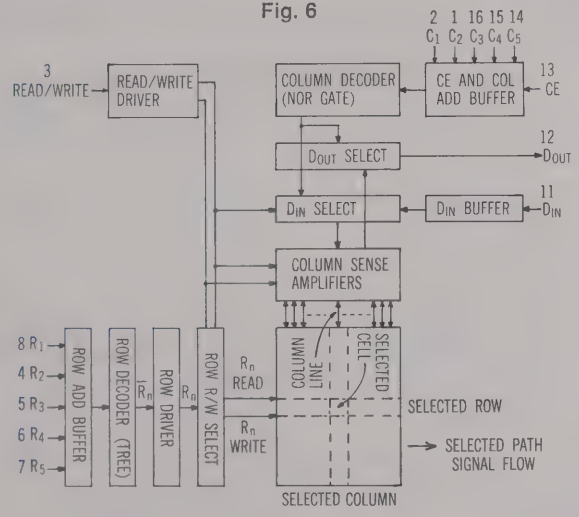


Fig. 7

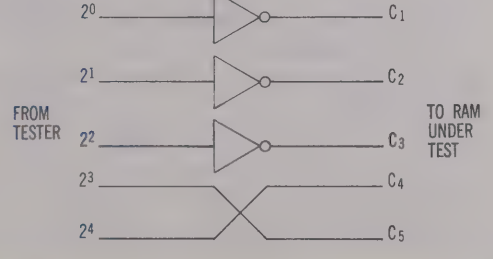
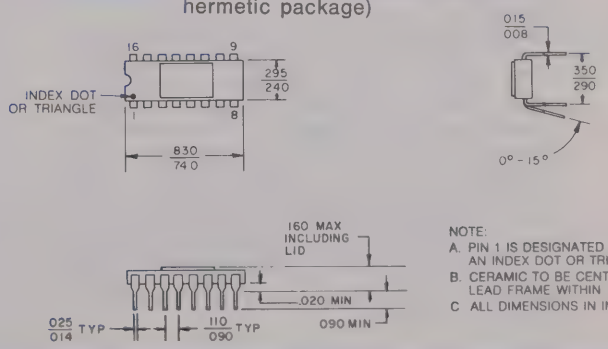


TABLE 1: FUNCTIONAL TESTS (SIMPLIFIED)

TEST DESC.	TEST SEQ.	OPER.	CHIP ENABLE	DATA INPUT	COMPARE DATA
Bit & Decoder Test[1]	First	Write	E	Parity	
	Next	Read	E		Parity
Column Shorts & No Write During Disable	First	Write	E	V-Bar	
	Next	Write	D	$\overline{\text{V-Bar}}$	
	Next	Read	E		V-Bar
Row Shorts, No Read During Disable, & Max. Power	First	Write	E	H-Bar	
	Next	Read	D	1	0
	Next	Read	E	0	H-Bar
Access Time, Refresh, Write Cycle, & Standby[1]	First	Write, Write	E	V-Bar, $\overline{\text{V-Bar}}$	
	Next	Delay	D	0	
	Next	Read	E		$\overline{\text{V-Bar}}$
Disturb Test	First	Write Row of 1's	E	1	
	Next	Write Adj. Row with 0's	E	0	
	Next	Continue Writing Same Row for Max. Refresh Delay	E	0	
	Next	Read original Row of 1's	E		1

1. Test performed as shown and repeated with complementary data.

PACKAGE (16-lead ceramic dual-in-line hermetic package)



NOTE:
A. PIN 1 IS DESIGNATED BY AN INDEX DOT OR TRIANGLE
B. CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN .020"
C. ALL DIMENSIONS IN INCHES

ORDERING INFORMATION

MK 4006 P: 1024x1 RAM/w/400 ns access time
MK 4008 P: 1024x1 RAM/w/500 ns access time
MK 4006-6 P: Power-down version of MK 4006 P
MK 4008-6 P: Power-down version of MK 4008 P

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... +0.3 to −20V

Operating Temperature ..... 0°C to +70°C

Storage Temperature Range ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS

(0° C ≤ T_A ≤ 70°C)

	PARAMETER	MK 4006,-6P — MK 4008,-6P MIN	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+4.75	+5.25	V	
V_{DD}	Supply Voltage	−11.4	−12.6	V	
V_{IL}	Input Voltage, Logic 0		+0.8	V	
V_{IH}	Input Voltage, Logic 1	V_{SS}−1	V_{SS}	V	
V_{SB}	Standby Supply Voltage (Fig. 4)	V_{SS}−4	V_{SS}−6	V	Note 1

RECOMMENDED AC OPERATING CONDITIONS[2]

(0° C ≤ T_A ≤ 70°C)

	PARAMETER	MK 4006 P MK 4006-6 P MIN	MAX	MK 4008 P MK 4008-6 P MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time (Fig. 1)	400		500		ns	
t_{WC}	Write Cycle Time (Fig. 2)	650		900		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{WP}	Write Pulse Width (Fig. 2)	250		400		ns ns	t_{AW}=400 ns t_{AW}=500 ns
t_{AW}	Address-to-Write Delay (Fig. 2)	400		500		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{DLD}	Data-to-Write Lead Time (Fig. 2)	300		400		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{RDLY}	Refresh Time (Fig. 3)		2		2	ms	See Note 3.
t_{CDPD}	Chip-Disable-to-Power-Down Delay (Fig. 4)	200		200		ns	See Note 1 See Note 4

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C ≤ T_A ≤ 70°C unless otherwise noted)

	PARAMETER	MK 4006 P MK 4006-6 P MIN	MAX	MK 4008 P MK 4008-6 P MIN	MAX	UNITS	NOTES
I_{SS}, I_{DD}	Supply Current: At T_A=0°C		30		30	mA	Output
	At T_A=70°C		24		24	mA	Open
P_{SDBY}	Power Dissipation, Standby		50		50	mW	$V_{SS}-V_{DD}$ = 5V; Note 1
I_{IH}	Input Current, Logic 1. Any Input	−5	+5	−5	+5	μA	$V_I=V_{SS}-1V$
I_{IL}	Input Current, Logic 0, Any Input	−5	+5	−5	+5	μA	V_I=0.8V
I_{OH}	Output Current, Logic 1	1.0		0.8		mA	Note 5
I_{OL}	Output Current, Logic 0		5		5	μA	

MK 4007 P

DS-4007571-2/MAY 1972

256 BIT
MOS Random Access Memory

MOSTEK CORPORATION

FEATURES:

- ☐ Versatile RAM can replace any existing 1101-type 256x1 MOS RAM pin for pin.
- ☐ Ion-implanted for superior performance.
- ☐ **Lower power dissipation:** TOTAL 250 mW max over entire temperature range.
- ☐ **Faster access time:** Typically 525 ns with V_D and V_{DD} at −9V.
- ☐ **Less temperature-sensitive:** specified over entire AMBIENT temperature range 0° to 75°C.
- ☐ **Tight control of output sink current capabilities:** made possible by use of depletion-mode transistors.
- ☐ **No restrictions** on address input sequence, skew, or rise and fall times.
- ☐ Full DTL/TTL compatibility.
- ☐ Wide power supply range: +5V; −6.5 to −15V.

APPLICATIONS:

Ideal for small buffer storage requiring low cost, superior performance, and bipolar compatibility, such as:

- ☐ Scratchpad memories
- ☐ Data link buffers
- ☐ Key-to-tape buffers
- ☐ Tape-to-printer buffers
- ☐ Editing memories.

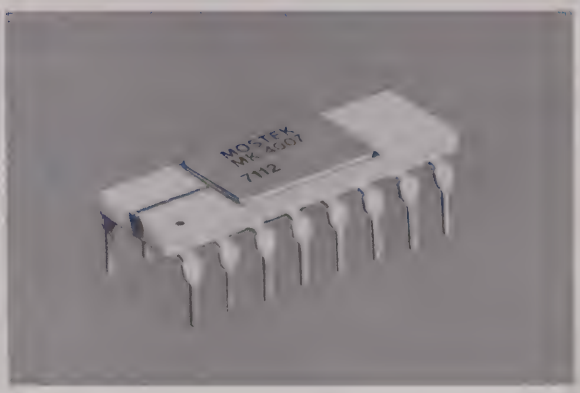
DESCRIPTION

Ion-implantation processes used in manufacturing the Mostek MK 4007 P Random Access MOS Memory result in a low-cost device with performance exceeding other industry types over the entire temperature and voltage supply ranges. It may be used to replace any existing 1101 type RAM pin for pin.

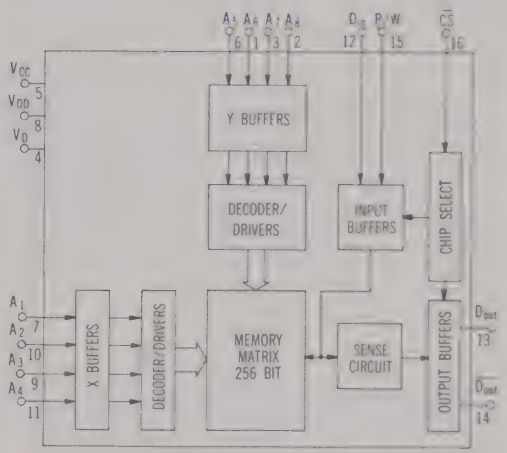
The depletion-load ion-implantation technique allows the fabrication of both depletion and enhancement mode transistors on the same chip. The result is not only superior operating characteristics within the region usually specified for devices of this type, but also wider operational areas without severe performance degradation. For example, while specifications for this device are given for V_D and V_{DD} from −7 to −13.2V, V_D and V_{DD} may actually range from −6.5 to −15 V (see DC Operating Conditions and Fig. 1). Access times are improved (see Fig. 2); power dissipation is reduced (see Fig. 3) and output sink current capabilities are improved (see Fig. 4). The device is less temperature-dependent (see Figures 5 and 6) and is specified over the *entire* ambient temperature range of 0° to 75°C.

The ion-implantation process also makes the MK 4007 P RAM fully TTL/DTL compatible at all inputs and outputs.

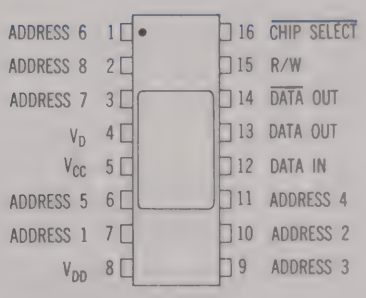
The 4007 P is a static memory, requiring no clocks or refreshing. Data is written into the address location by applying a logic "1" to the R/W input. Addressing the desired location, with the chip enabled and R/W at logic "0", provides a non-destructive read-out (NDRO) of true and complement data. A "Chip Select" allows output buffers to be open-circuited during disable time for wire ORing. All inputs are protected against static charge accumulation.



FUNCTIONAL DIAGRAM



PIN CONNECTIONS



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MOSTEK CORPORATION ®

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{CC} . . . . . + 0.3 V to −25 V
Operating Temperature Range (Ambient) . . . . . 0°C to +75°C
Storage Temperature Range (Ambient) . . . . . −55° to +150°C

DC OPERATING CONDITIONS

(Ambient Temperature Range: 0°C to +75°C)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
	V_{DD}	Supply Voltage	−6.5	−9.0	−15.0	V	See Fig. 1 for
	V_D	Supply Voltage	−6.5	−9.0	−15.0	V	V_D, V_{DD} differential
INPUTS	V_{IL}	Logic "0" Voltage, any input		0	+0.8	V	
	V_{IH}	Logic "1" Voltage, any input	V_{CC} −2.0	V_{CC}	V_{CC}+0.3	V	

ELECTRICAL CHARACTERISTICS

(Ambient Temperature Range: 0°C to +75°C. V_{CC} = +5 V ±5%;
$V_D = V_{DD}$ = −7 V to −13.2 V, unless otherwise specified.)

		PARAMETER	MIN	TYP(1)	MAX	UNITS	CONDITIONS
POWER	I_D	Supply Current. V_D		8.0	11.5	mA	$V_D = V_{DD}$ = −9V ±5% Outputs open-circuited.
	I_{DD}	Supply Current, V_{DD}		4.0	6.5	mA	
	P_D	Power Dissipation, Total		170	250	mW	
	I_D	Supply Current. V_D			13.0	mA	$V_D = V_{DD}$ = −13.2 V V_{CC} = +5.25 V Outputs open-circuited.
	I_{DD}	Supply Current, V_{DD}			7.0	mA	
	P_D	Power Dissipation, Total			370	mW	
	P_{SDBY}	Power Dissipation, Standby		30	75	mW	$V_D = V_{CC}$; V_{DD} = −9V ±5%
INPUTS	$I_{I(L)}$	Input Leakage Current			1.0	μA	V_{IN} = 0 V, T_A = 25°C
	C_{IN}	Input Capacitance, Any Logic Input		7	10	pF	T_A = 25°C, F. meas. = 1 MHz; Tested input = V_{CC}
	$C_{V(D)}$	Capacitance, V_D Power Supply		35		pF	
OUTPUTS	I_{OL}	Output Current, Logic "0"	3.2	5.6		mA	V_O = +0.40 V
	I_{OH}	Output Current, Logic "1"	−1.0	−4.2		mA	V_O = +2.6 V
	I_{OLC}	Output Clamp Current, Logic "0"			8.0	mA	V_O = −1.0 V
	$I_{O(L)}$	Output Leakage Current			1.0	μA	$V_O = V_{CC}$ −5V; $\overline{CS}$ = Logic 1; T_A = 25°C.
	C_{OUT}	Output Capacitance		7	10	pF	T_A = 25°C; F meas. = 1 MHz; $V_O = V_{CC}$

NOTES:

(1) Typical values at V_{CC} = +5 V, $V_D = V_{DD}$ = −9.0 V*, T_A = 25°C.
(*Except Standby Power)

TIMING

(Ambient Temperature Range: 0°C to 75°C; $V_{CC} = +5$ V $\pm 5\%$; $V_D = V_{DD} = -7$V to -13.2 V, unless otherwise specified. See Notes 1 and 2.)

		PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
OPERATING CONDITIONS	t_{wc}	Write Cycle Time	700			ns	
	t_{wd}	Write Set-up Delay	300			ns	
	t_{wp}	Write Pulse Width	400			ns	
	t_{did}	Data Lead Time	300			ns	
	t_{dig}	Data Lag Time	0			ns	
	t_{cw}	Chip Select Pulse Width	400			ns	
DYNAMIC CHAR.	t_{ACC}	Access Time		525	900	ns	$V_D = V_{DD} = -9$V $\pm 5\%$.
	t_{RC}	Read Cycle Time			800	ns	(See Note 3.)
	t_{ACC}	Access Time			1.0	μs	$V_D = V_{DD} = -7$V to -13.2V.
	t_{RC}	Read Cycle Time			900	ns	(See Note 3.)
	t_{OH}	Data Output Hold Time	100			ns	
	t_{CSE}	Chip-Select-to-Output Enable			300	ns	
	t_{CSD}	Chip-Select-to-Output Disable			300	ns	

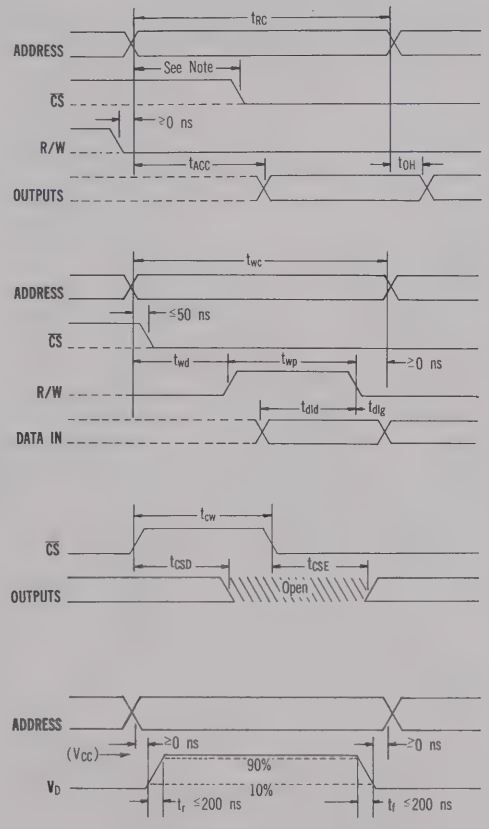
NOTES:

(1) All measurements to the 1.5 V level; inputs for test are 0 to 5 V and $\leq$10 ns rise and fall times; output is loaded with 1 TTL and approx. 20 pF.

(2) R/W should be brought to logical "0" whenever address bits are changed; however, there are no restrictions on rise and fall times of address bits, nor on the sequence (or skew) of address bit changes.

(3) Read Cycle may be "pipe-lined," i.e., the minimum hold time (t_{OH}) may be subtracted from the maximum access time (t_{ACC}).

TIMING



READ CYCLE

Reading is accomplished with R/W (Read/Write) and $\overline{CS}$ (Chip Select) at logical "0."

NOTE: $\overline{CS}$ logical "1" overlap time shown must be 300 ns (max t_{CSE}) less than the desired access time; e.g., if desired access time $t_{ACC} = 1.2$ μs, then $\overline{CS}$ should go to logical "0" no later than 900 ns following address change.

WRITE CYCLE

Writing is accomplished with R/W at logical "1" and $\overline{CS}$ at logical "0." $\overline{CS}$ at logical "1" may overlap the address change as much as 50 ns. R/W may be taken to logical "0" coincidentally with an address change, but should not overlap an address change while in the logical "1" state.

CHIP SELECT

Chip Select at logical "1" causes the normal push-pull output buffers to be open-circuited for purposes of wire-ORing. The Chip Select may be used to access the memory at a faster rate by maintaining a constant address and selecting individual chips with the Chip Select input.

POWER SWITCHING

During standby operation the MK 4007 P will dissipate only 30 mW of power (typically) if the peripheral power supply, V_D, is reduced to V_{CC}. The R/W input may be maintained at logical "0" or "1"; however, if R/W is at logical "1," Chip Select should also be logical "1" (to disable chip during standby operation). With the return of power, either read or write cycles may commence as described above.

TYPICAL PERFORMANCE CURVES

FIG. 1: POWER SUPPLY OPERATING REGION & DIFFERENTIAL

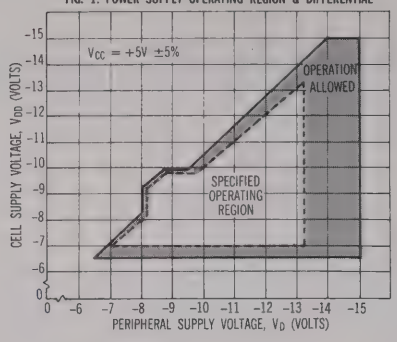


FIG. 2: ACCESS TIME VS SUPPLY VOLTAGE, (V_D)

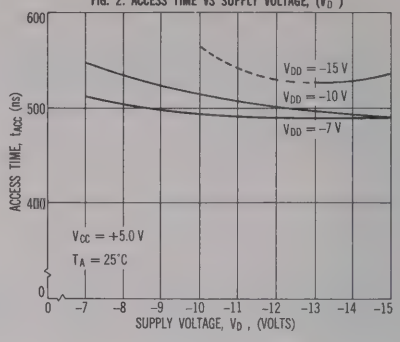


FIG. 3: TOTAL POWER DISSIPATION, (P_D), VS SUPPLY VOLTAGE, (V_D and V_{DD})

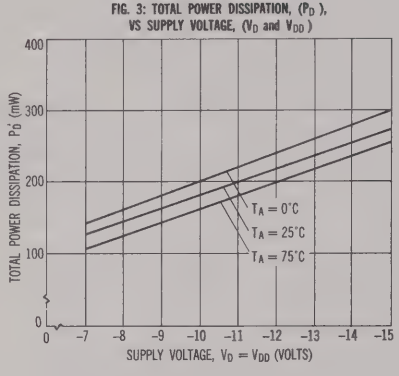


FIG. 4: OUTPUT CURRENT VS OUTPUT VOLTAGE

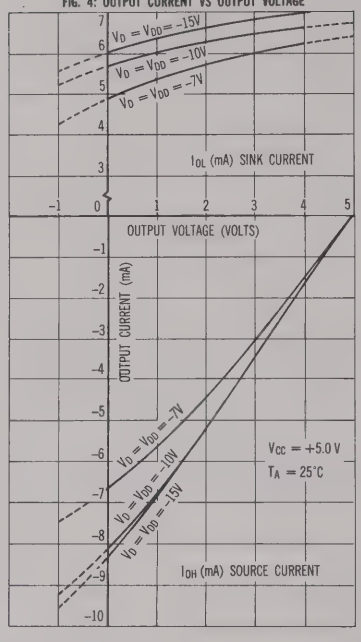

V_D = V_{DD} = −15V
V_D = V_{DD} = −10V
V_D = V_{DD} = −7V
I_{OL} (mA) SINK CURRENT
OUTPUT VOLTAGE (VOLTS)
OUTPUT CURRENT (mA)
V_{CC} = +5.0 V
T_A = 25°C
I_{OH} (mA) SOURCE CURRENT

FIG. 5: OUTPUT CURRENT VS AMBIENT TEMPERATURE

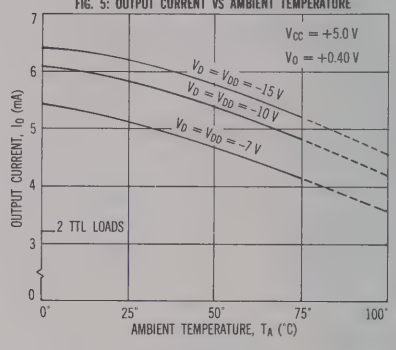


FIG. 6: WORST-CASE ACCESS TIME VS SUPPLY VOLTAGE (At Various Capacitances and Ambient Temperatures)

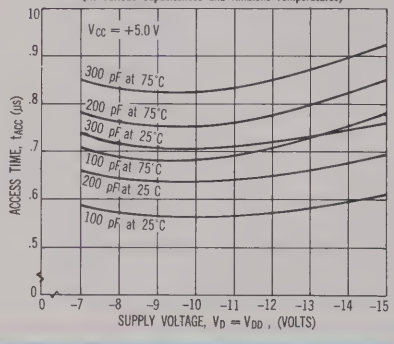

V_{CC} = +5.0 V
300 pF at 75°C
200 pF at 75°C
300 pF at 25°C
100 pF at 75°C
200 pF at 25°C
100 pF at 25°C
ACCESS TIME, t_{ACC} (µs)
SUPPLY VOLTAGE, V_D = V_{DD}, (VOLTS)

FIG. 7: SUPPLY CURRENT, (I_D and I_{DD}), VS SUPPLY VOLTAGE (V_D and V_{DD})

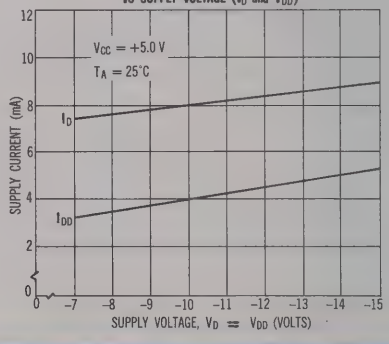
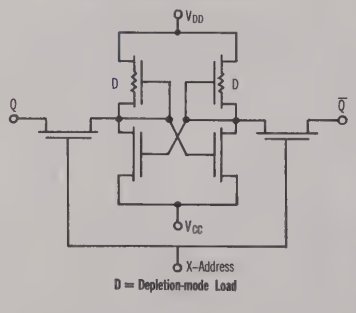
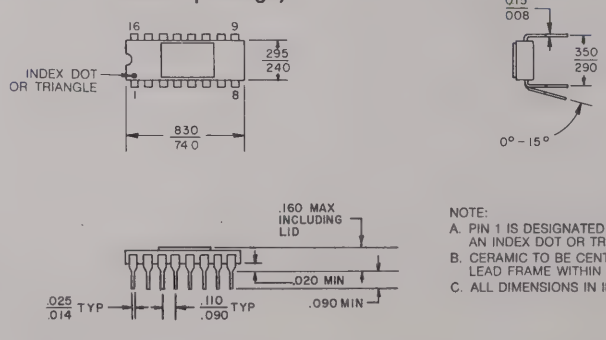


FIG. 8: MK 4007 P MEMORY CELL



PACKAGE (16-lead ceramic dual-in-line hermetic package)



NOTE:
A. PIN 1 IS DESIGNATED BY AN INDEX DOT OR TRIANGLE
B. CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN .020"
C. ALL DIMENSIONS IN INCHES

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SUPPLEMENT to MK 4007-4 P

256-BIT

MOS Random Access Memory

MOSTEK

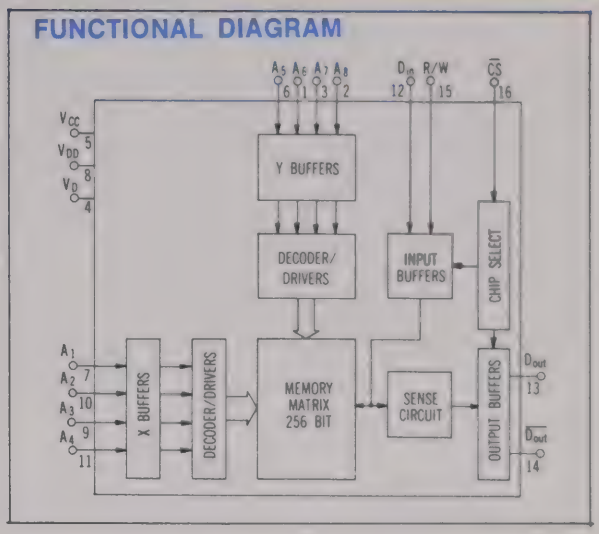
DSS4007-4-672/JUNE 1972

- Low-cost 256x1 RAM in 16-pin package.
- Identical with Mostek's MK 4007 P in all specifications except output current

DESCRIPTION

This economical version of Mostek's 256x1 bit RAM is identical with the MK 4007 P in all electrical characteristics except output current. Performance, operating conditions, timing characteristics, package, and all other specifications are identical with the MK 4007 P. See the MK 4007 P Data Sheet for additional information.

FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

(Ambient Temperature Range: 0°C to +75°C. V_{CC} = +5 V ±5%; V_D = V_{DD} = −7 V to −13.2 V, unless otherwise specified.)

		PARAMETER	MIN	TYP(1)	MAX	UNITS	CONDITIONS
POWER	I_D	Supply Current, V_D		8.0	11.5	mA	V_D = V_{DD} = −9 V ±5%
	I_{DD}	Supply Current, V_{DD}		4.0	6.5	mA	Outputs open-circuited.
	P_D	Power Dissipation, Total		170	250	mW	
	I_D	Supply Current, V_D			13.0	mA	V_D = V_{DD} = −13.2 V
	I_{DD}	Supply Current, V_{DD}			7.0	mA	V_{CC} = +5.25 V
	P_D	Power Dissipation, Total			370	mW	Outputs open-circuited.
	P_{SDBY}	Power Dissipation, Standby		30	75	mW	V_D = V_{CC}; V_{DD} = −9V ±5%
INPUTS	$I_{I(L)}$	Input Leakage Current			1.0	μA	V_{IN} = O V, T_A = 25°C
	C_{IN}	Input Capacitance, Any Logic Input		7	10	pF	T_A = 25°C, F. Meas. =
	$C_{V(D)}$	Capacitance, V_D Power Supply		35		pF	1 MHz; Tested input = V_{CC}
OUTPUTS	I_{OL}	Output Current, Logic "0": @ T_A = 25°C	3.0	5.6		mA	V_O = +0.40 V; V_{CC} = 5.0 V ±5%
		Output Current, Logic "0": @ T_A = 70°C	2.0			mA	V_O = +0.40 V; V_D = V_{DD} = −9.0 V
	I_{OH}	Output Current, Logic "1"	−1.0	−4.2		mA	V_O = +2.6 V; ±10%
	I_{OLC}	Output Clamp Current, Logic "0"			8.0	mA	V_O = −1.0 V
	$I_{O(L)}$	Output Leakage Current			1.0	μA	V_O = V_{CC} −5V; $\overline{CS}$ = Logic 1; T_A = 25°C.
	C_{OUT}	Output Capacitance		7	10	pF	T_A = 25°C; F meas. = 1 MHz; V_O = V_{CC}

NOTES:

(1) Typical values at V_{CC} = +5 V, V_D = V_{DD} = −9.0 V*, T_A = 25°C.
(*Except Standby Power)

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SUPPLEMENT 1 MK 4007-4 P

256-BIT

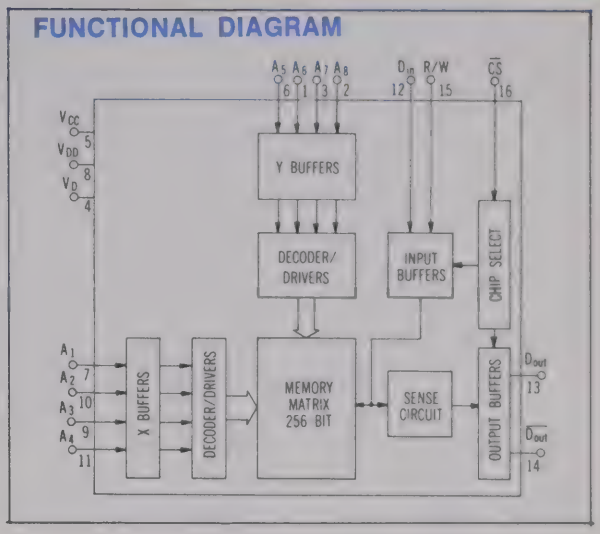
MOS Random Access Memory

MOSTEK

DSS4007-4-672/JUNE 1972

- Low-cost 256x1 RAM in 16-pin package.
- Identical with Mostek's MK 4007 P in all specifications except output current

FUNCTIONAL DIAGRAM



DESCRIPTION

This economical version of Mostek's 256x1 bit RAM is identical with the MK 4007 P in all electrical characteristics except output current. Performance, operating conditions, timing characteristics, package, and all other specifications are identical with the MK 4007 P. See the MK 4007 P Data Sheet for additional information.

ELECTRICAL CHARACTERISTICS

(Ambient Temperature Range: 0°C to +75°C. V_{CC} = +5 V ±5%; V_D = V_{DD} = −7 V to −13.2 V, unless otherwise specified.)

		PARAMETER	MIN	TYP(1)	MAX	UNITS	CONDITIONS
POWER	I_D	Supply Current, V_D		8.0	11.5	mA	V_D = V_{DD} = −9 V ±5%
	I_{DD}	Supply Current, V_{DD}		4.0	6.5	mA	Outputs open-circuited.
	P_D	Power Dissipation, Total		170	250	mW	
	I_D	Supply Current, V_D			13.0	mA	V_D = V_{DD} = −13.2 V
	I_{DD}	Supply Current, V_{DD}			7.0	mA	V_{CC} = +5.25 V
	P_D	Power Dissipation, Total			370	mW	Outputs open-circuited.
	P_{SDBY}	Power Dissipation, Standby		30	75	mW	V_D = V_{CC}; V_{DD} = −9V ±5%
INPUTS	$I_{I(L)}$	Input Leakage Current			1.0	μA	V_{IN} = O V, T_A = 25°C
	C_{IN}	Input Capacitance, Any Logic Input		7	10	pF	T_A = 25°C, F. Meas. =
	$C_{V(D)}$	Capacitance, V_D Power Supply		35		pF	1 MHz; Tested input = V_{CC}
OUTPUTS	I_{OL}	Output Current, Logic "0": @ T_A = 25°C	3.0	5.6		mA	V_O = +0.40 V (V_{CC} = 5.0 V ±5%)
		Output Current, Logic "0": @ T_A = 70°C	2.0			mA	V_O = +0.40 V (V_D = V_{DD} = −9.0 V
	I_{OH}	Output Current, Logic "1"	−1.0	−4.2		mA	V_O = +2.6 V ±10%
	I_{OLC}	Output Clamp Current, Logic "0"			8.0	mA	V_O = −1.0 V
	$I_{O(L)}$	Output Leakage Current			1.0	μA	V_O = V_{CC} −5V; $\overline{CS}$ = Logic 1; T_A = 25°C.
	C_{OUT}	Output Capacitance		7	10	pF	T_A = 25°C; F meas. = 1 MHz; V_O = V_{CC}

NOTES:

(1) Typical values at V_{CC} = +5 V, V_D = V_{DD} = −9.0 V*, T_A = 25°C.
(*Except Standby Power)

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MOS Special Products

MOSTEK CORPORATION

PRELIMINARY

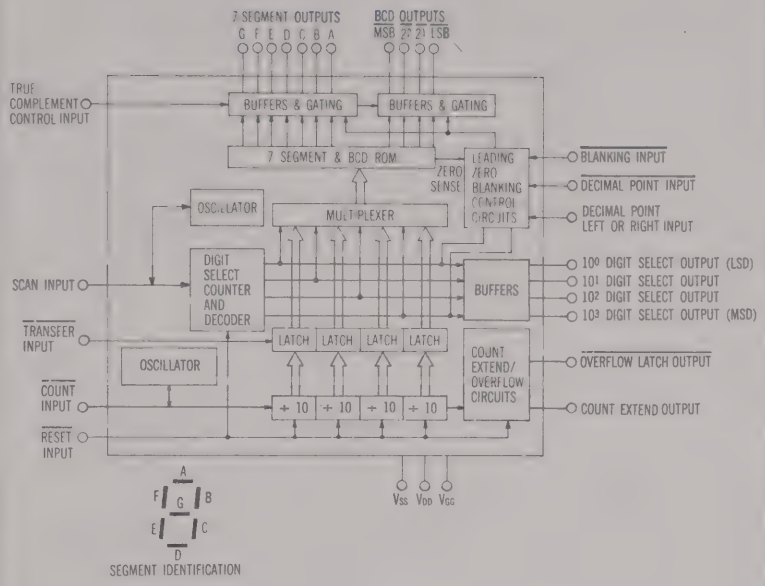
MK 5002 P | MK 5003 P
MK 5004 P | MK 5005 P

PDS-50021071-2/JUL 1972

MOS 4-Digit Counter/Display Decoder

MOSTEK

FUNCTIONAL DIAGRAM



GENERAL DESCRIPTION

The MK 5002 P is an ion-implanted, P-channel MOS four-decade synchronous counter with latches, multiplexing circuits, and a read-only memory programmed for seven-segment outputs and BCD outputs. In addition, many on-chip control circuits provide flexibility of use with a minimum of external components. The device will count and display from 0 through 9,999.

Low threshold voltages for DTL/TTL compatibility are achieved through Mostek's ion-implantation process. Enhancement mode, as well as depletion-mode, devices are fabricated on the chip, allowing it to operate from a single +5V power supply. Depletion-mode technology also allows the entire circuit to operate on less than 25 mW of power.

Custom programming of the output read-only memory is available if other than BCD and seven-segment outputs are required. Any output code utilizing up to eleven available output pins, as in segmented-tube readouts, may be programmed by a single mask change.

TRUTH TABLES

INPUT TRUTH TABLE

Input	Logic Condition to Activate
$\overline{\text{Count}}$	Negative Edge
$\overline{\text{Reset}}$	0
$\overline{\text{Transfer}}$	0
Scan	0 (Negative Edge)
True/Complement	1 = True Data 0 = Complementary Data
$\overline{\text{Decimal Point}}$	0
$\overline{\text{Blanking}}$	0
Decimal Point Left or Right	1 = Left 0 = Right

7-SEGMENT & BCD OUTPUTS TRUTH TABLE

	DISPLAY SEGMENT							BCD			
	a	b	c	d	e	f	g	$\overline{\text{MSB}}$	$\overline{2^2}$	$\overline{2^1}$	$\overline{\text{LSB}}$
Digit 0	0	0	0	0	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	0
2	0	0	1	0	0	1	0	1	1	0	1
3	0	0	0	0	1	1	0	1	1	0	0
4	1	0	0	1	1	0	0	1	0	1	1
5	0	1	0	0	1	0	0	1	0	1	0
6	0	1	0	0	0	0	0	1	0	0	1
7	0	0	0	1	1	1	1	1	0	0	0
8	0	0	0	0	0	0	0	0	1	1	1
9	0	0	0	0	1	0	0	0	1	1	0

TRUE DATA OUT: Logic 0, Segment On, Low
Logic 1, Segment Off, High

TRUTH TABLE, OTHER OUTPUTS

Output	True Logic State	Time of Occurrence
Digit Select Outputs	1	One-of-four, following Scan Input rising edge; all off when Scan Input is low.
$\overline{\text{Overflow Latch}}$	0	Occurs on the 10,000th Count Input following a reset. Remains true until an external reset is accomplished.
Count Extend	1	Occurs each time the counter state attains 9,999 count. Remains true only until the next Count Input or Reset occurs (when the counter returns to 0,000).

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RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
T_A	Operating Temperature Range	0		75	°C	
V_{SS}	Supply Voltage	4.5		7.5	V	1, 2
V_{GG}	Supply Voltage	V_{DD}		-14.0	V	1, 2

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 5\%$; $V_{GG} = V_{DD} = 0$ V; 0° C $\leq T_A \leq$ 75° C unless otherwise noted)

		PARAMETER	MIN	TYP	MAX	UNITS	NOTES
D. C. CHARACTERISTICS	V_{IL}	Input Voltage, Logic 0 (Low)		V_{DD}	V_{SS}-4	V	
	V_{IH}	Input Voltage, Logic 1 (High)	V_{SS}-1	V_{SS}	V_{SS}+0.3	V	3
	I_{SS}	Supply Current, V_{SS}		2.5	5.0	mA	4, Inputs open
	I_{GG}	Supply Current, V_{GG}		0.2	0.5	mA	V_{GG}=-12V
	C_{in}	Input Capacitance		3	10	pF	T_A = 25°C
	I_I	Input Current, Logic 0, Count Input			1.6	mA	5
		Scan Input			1.6	mA	5
		Decimal Point Input			1.0	µA	
		Other Logic Inputs			1.0	mA	
	I_{OL}	Output Current, Logic 0	0.6			mA	6, V_{GG}=-12V
	I_{OH}	Output Current, Logic 1	0.6			mA	6, V_{GG}=-12V
	V_{OL}	Output Voltage, Logic 0	V_{DD}+0.2			V	4
	V_{OH}	Output Voltage, Logic 1	V_{SS}-0.2			V	4
DYNAMIC CHARACTERISTICS	f_{CI}	Count Input Frequency	DC		250	KHz	
	f_{SI}	Scan Input Frequency	DC		50	KHz	
	t_{RD}	Reset to Any Output Delay			15	µs	
	t_{PW}	Logic 0 Pulse Width, Reset Input	1.0			µs	
		Count Input	1.0			µs	
		Scan Input	10.0			µs	
		Transfer Input	2.5			µs	
	t_{PH}	Logic 1 Time, Count Input	3.0			µs	
		Scan Input	10.0			µs	
	t_{SD}	Scan to Output Disable Time					
		Digit Select Outputs			15	µs	7
		All Data Outputs			15	µs	7
	t_{SE}	Scan to Output Enable Time					
		Digit Select Outputs			15	µs	8
		All Data Outputs			15	µs	8
	t_{CE}	Count Input to Count Extend Delay to 1 or 0			15	µs	9
	t_{OF}	Count Input to Overflow Delay (On)			15	µs	9
	t_{ROF}	Reset Input to Overflow Delay (Off)			5	µs	

NOTES:
1. V_{DD} = 0 V
2. V_{SS}/V_{GG} differential no more than 25 V.
3. Internal pull-up resistors (approx 10 K Ohm) are provided at all inputs other than Count Input, Scan Input, & Decimal Point Input.
4. V_{GG} = -12V ± 10%. Outputs open.
5. Measurement made at $V_I = V_{SS}$ - 4.0 V. This condition is sufficient to represent a logic 0 and hold off or override the internal oscillators. Maximum current at V_I = +0.4V is 1.6 mA. 400 µA source current at V_{SS}-1.0 is sufficient to represent a logic 1 and hold off or override the internal oscillators.
6. I_{OL} measured at $V_O = V_{SS}$ - 0.75 V. I_{OH} measured at $V_O = V_{DD}$ + 0.75 V. (See MK 5002 P Application Note for output characteristics.)
7. Delay measured from the negative edge of the Scan Input.
8. Delay measured from the rising edge of the Scan Input.
9. Delay measured from the negative edge of the Count Input.

DESCRIPTION OF OPERATION

Refer to the MK 5002 P Application Report for information concerning the use of various functions described in the following information.

COUNTER LOGIC & TIMING

The decade counters are synchronously incremented on the negative edge of the Count Input. The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} supply.

SCAN CONTROL LOGIC & TIMING

The Digit Select Counter is incremented by the negative edge of the Scan Input. During the time the Scan Input is at 0, the 7-segment and BCD outputs and all Digit Select outputs are forced to the OFF condition and remain so until the Scan Input returns to logic 1. Built-in synchronization logic ensures that both the 7-segment and BCD data for the selected latch are valid prior to enabling the corresponding Digit Select output.

The counter's output is a one-of-four, scanning from MSD (Most Significant Digit) to LSD (Least Significant Digit), enabling one quad latch output to be decoded into 7-segment data and presenting a logic 1 to the corresponding Digit Select output.

The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} supply.

TRANSFER LOGIC & TIMING

While the Transfer Input is at logic 0, data in the decade counters is transferred to the static storage latches. This input may be left at 0 for a continuous transfer-and-display mode, or may be pulsed periodically to store only on command.

Termination of a transfer command occurs when the input is taken to a logic 1 and the next Count Input negative edge occurs. This allows asynchronous Count and Transfer operation since the transfer is terminated prior to incrementing the counters. This means that a Count Input negative edge must follow a Transfer command before a Reset is applied to prevent transfer of invalid data. An external Reset command must be delayed at least one Count Input pulse following a Transfer. External transfer should terminate at least 1 μs prior to this Count negative edge and Reset should occur no sooner than 1 μs following that edge.

RESET CONTROL

The decade counters are reset to 0,000 when the Reset Input is at logic 0. The Reset at logic 0 also forces the Scan to the MSD output and resets the Overflow output to a logic 1 (if previously latched to logic 0). It maintains these conditions as long as the logic 0 is present at the Reset, and overrides all other associated inputs. As indicated previously, decade counters should not be Reset until a Transfer has been terminated.

Since the Reset Input resets the Scan Counter to MSD the scan rate must be much faster than the Reset rate to allow the lesser significant digits to be enabled. Therefore, F_{Scan} must be much greater than four times F_{Reset}.

Ideally, the Reset pulse should also be made narrow, to prevent its duration from causing the MSD to be ON much longer than the other digits and thus appear to be brighter.

LEADING ZERO BLANKING

At the start of each MSD to LSD scan, blanking of leading zeros occurs until the first non-zero number occurs in the display or the Decimal Point Input is clocked. Any number following will be displayed. Leading zero blanking does not affect the BCD outputs or the LSD in the display which is displayed even if zero.

The Decimal Point Input should be brought to logic 0 at the time the character is enabled that contains the decimal point. A convenient method of accomplishing this is to route the Digit Select outputs through a range select switch, invert the resulting output, and feed it to the Decimal Point Input.

Leading zero blanking may be inhibited by wiring the Decimal Point Input to ground.

OTHER INPUTS

The Blanking Input at logic 0 forces the 7-segment outputs to the off-state and the BCD to the equivalent of the number zero. This condition is maintained on a DC basis as long as Blanking is 0. The Digit Select outputs continue to operate at the scan rate as described.

A True/Complement control inverts both BCD and 7-segment outputs when at logic 0. A combination of blanking at 0 and True/Complement at 0 would produce all segments ON for a lamp test.

DECIMAL POINT LEFT OR RIGHT

The control allows the use of displays with the decimal point physically located on the left or right of the numeral. Logic 1 is decimal-point-left; logic 0 is decimal-point-right. In the right mode, even though the Decimal point input is clocked, unblanking is delayed until the following digit is enabled.

OUTPUTS

All output buffers on the MK 5002 family are push-pull. A negative power supply terminal, V_{GG}, is provided to increase the drive capabilities of these output buffers. Since the V_{GG} supply is connected only to these output buffers, it has no effect on any other device characteristics.

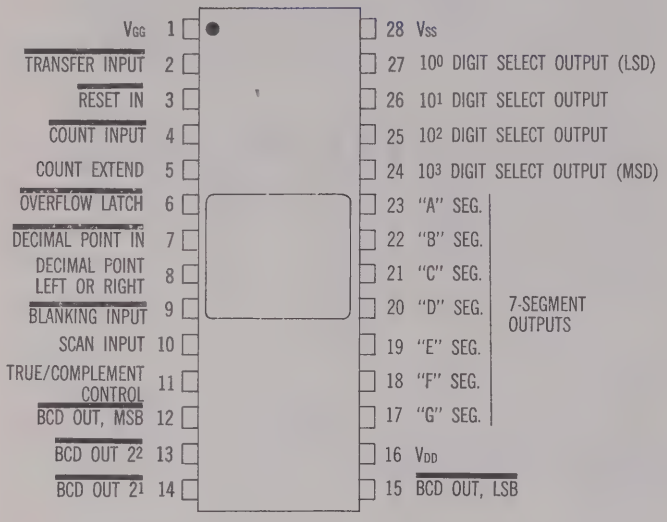
Output characteristics are covered in the MK 5002 Application Report which illustrates the effects of V_{GG} with current to be expected at various output voltages.

The outputs are designed to drive directly to the base of common-emitter transistors, so that output voltage is clamped or maintained at a potential where the MK 5002 P is able to sink or source its greater amount of current.

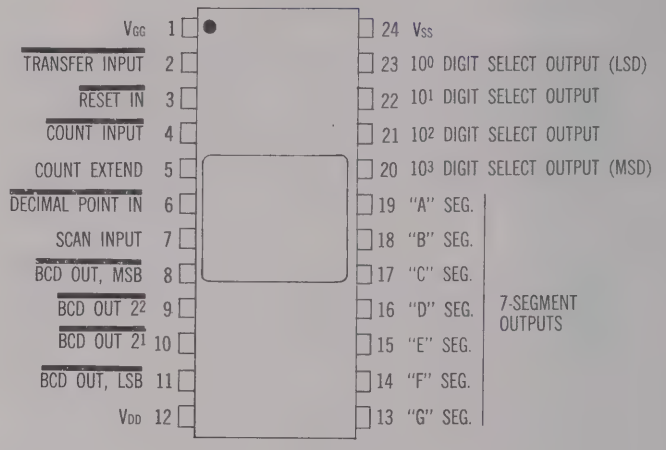
PIN CONNECTIONS

The MK 5002 P is available in both a 28-pin dual-in-line package and a 24-pin dual-in-line package. Only the 28-pin package contains all available functions. Some of the functions shown on the block diagram are bondable options in the 24-pin packages as illustrated below. See MK 5007 P data sheet for 16-pin version.

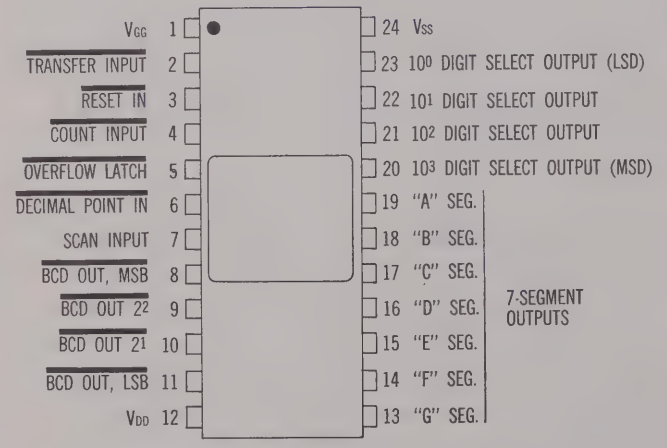
MK 5002 P PIN CONNECTIONS



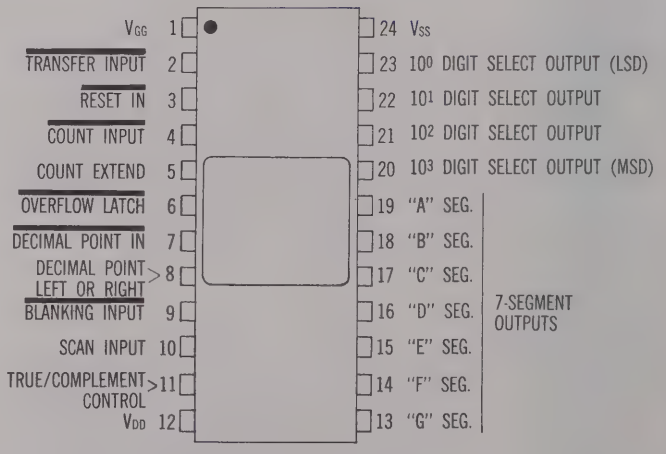
MK 5003 P PIN CONNECTIONS



MK 5004 P PIN CONNECTIONS



MK 5005 P PIN CONNECTIONS



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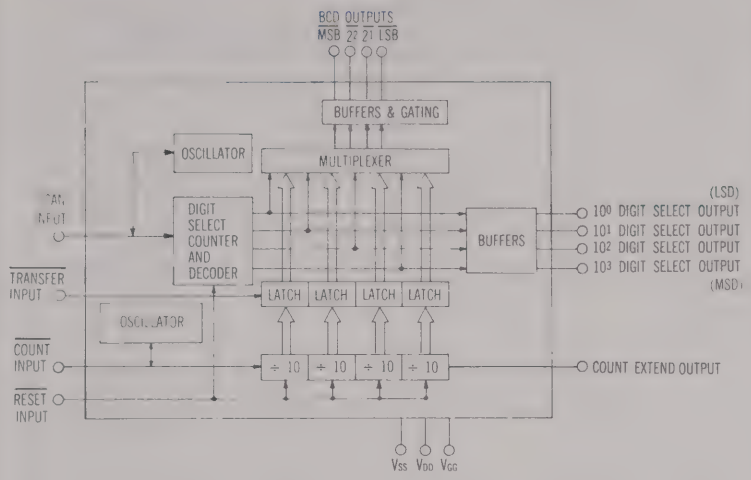
PRELIMINARY **MK 5007 P**

MOS
4-Digit Counter/Display Decoder

MOSTEK

PY-5007572-2/JUL 1972

FUNCTIONAL DIAGRAM



GENERAL DESCRIPTION

The MK 5007 P is an ion-implanted, P-channel MOS four-decade synchronous counter with latches and multiplexing circuitry for BCD outputs. It is a member of Mostek's family of 4-digit counter/display circuits.

The MK 5007 P provides a means of counting up to 9999, transferring the count into latches without interrupting the counting operation, and supplying the latched information to the outputs one decade at a time. Scanning is controlled by the Scan Input which increments a one-of-four counter on its negative edge, thereby scanning the latches from MSD (Most Significant Digit) to LSD (Least Significant Digit).

Low threshold voltages for DTL/TTL compatibility are achieved through Mostek's ion-implantation process. Enhancement-mode, as well as depletion-mode, devices are fabricated on the chip, allowing it to operate from a single +5V power supply. Depletion-mode technology also allows the entire circuit to operate on less than 25 mW of power.

TRUTH TABLES

INPUT TRUTH TABLE	
Input	Logic Condition to Activate
$\overline{\text{Count}}$	Negative Edge
$\overline{\text{Reset}}$	0
$\overline{\text{Transfer}}$	0
Scan	0 (Negative Edge)

OUTPUT TRUTH TABLES					
		BCD OUTPUTS			
Scan	Digit	$\overline{\text{MSB}}$	$\overline{2^2}$	$\overline{2^1}$	$\overline{\text{LSB}}$
1	0	1	1	1	1
1	1	1	1	1	0
1	2	1	1	0	1
1	3	1	1	0	0
1	4	1	0	1	1
1	5	1	0	1	0
1	6	1	0	0	1
1	7	1	0	0	0
1	8	0	1	1	1
1	9	0	1	1	0
0	0	1	1	1	1

TRUTH TABLE, OTHER OUTPUTS		
OTHER OUTPUTS	True Logic State	Time of Occurrence
Digit Select Outputs	1	One-of-four, following Scan Input rising edge; all off when Scan Input is low.
Count Extend	1	Occurs each time the counter state attains 9,999 count. Remains true only until the next Count Input or Reset occurs (when the counter returns to 0,000).

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RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
T_A	Operating Temperature Range	0		75	°C	
V_{SS}	Supply Voltage	4.5		7.5	V	1
V_{GG}	Supply Voltage	V_{DD}		-13.2	V	1

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 5\%$; $V_{GG} = V_{DD} = 0V$; $0°C \leq T_A \leq 75°C$ unless otherwise noted.)

		PARAMETER	MIN	TYP	MAX	UNITS	NOTES
D. C. CHARACTERISTICS	V_{IL}	Input Voltage, Logic 0 (Low)		V_{DD}	$V_{DD}+0.8$	V	
	V_{IH}	Input Voltage, Logic 1 (High)	$V_{SS}-1$	V_{SS}	$V_{SS}+0.3$	V	2
	I_{SS}	Supply Current, V_{SS}		2.5	5.0	mA	3, Inputs open
	I_{GG}	Supply Current, V_{GG}		0.2	0.5	mA	V_{GG}=-12V
	C_{in}	Input Capacitance		3	10	pF	T_A=25°C; f=1MHz
	I_I	Input Current, Logic 0, Count Input			1.6	mA	4
		Scan Input			1.6	mA	4
		Other Logic Inputs			1.0	mA	
	I_{OL}	Output Current, Logic 0	0.6			mA	5, V_{GG}=-12V
	I_{OH}	Output Current, Logic 1	0.6			mA	5, V_{GG}=-12V
	V_{OL}	Output Voltage, Logic 0	$V_{DD}+0.2$			V	3
	V_{OH}	Output Voltage, Logic 1	$V_{SS}-0.2$			V	3
DYNAMIC CHARACTERISTICS	f_{CI}	Count Input Frequency	DC		250	KHz	
	f_{SI}	Scan Input Frequency	DC		50	KHz	
	t_{RD}	Reset to Any Output Delay			15	µs	
	t_{PW}	Logic 0 Pulse Width, Reset Input	1.0			µs	
		Count Input	1.0			µs	
		Scan Input	10.0			µs	
		Transfer Input	2.5			µs	
	t_{PH}	Logic 1 Time, Count Input	3.0			µs	
		Scan Input	10.0			µs	
	t_{SD}	Scan to Output Disable Time					
		Digit Select Outputs			15	µs	6
		All Data Outputs			15	µs	6
	t_{SE}	Scan to Output Enable Time					
		Digit Select Outputs			15	µs	7
		All Data Outputs			15	µs	7
	t_{CE}	Count Input to Count Extend Delay to 1 or 0			15	µs	8

NOTES

1. V_{DD} = 0 V
2. Internal pull-up resistors (approx 10 K Ohm) are provided at all inputs other than Count Input and Scan Input.
3. V_{GG} = -12V ± 10%. Outputs open.
4. Measurement made at $V_I = V_{SS} - 4.0$ V. This condition is sufficient to represent a logic 0 and hold off or override the internal oscillators. Maximum current at V_I = +0.4V is 1.6 mA. 400 µA source current at V_{SS}-1.0 is sufficient to represent a logic 1 and hold off or override the internal oscillators.
5. I_{OL} measured at $V_O = V_{SS} - 0.75$ V. I_{OH} measured at $V_O = V_{DD} + 0.75$ V. (See MK 5002 P Application Note for output characteristics.)
6. Delay measured from the negative edge of the Scan Input.
7. Delay measured from the rising edge of the Scan Input.
8. Delay measured from the negative edge of the Count Input.

DESCRIPTION OF OPERATION

(Further information on the operation of Mostek's family of 4-digit Counter/Decoders may be found in the MK 5002 P Application Report.)

COUNTER LOGIC & TIMING

The Decade counters are synchronously incremented on the negative edge of the Count Input. The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{SS}.

SCAN CONTROL LOGIC & TIMING

The Digit Select Counter is incremented by the negative edge of the Scan Input. During the time the Scan Input is at 0, BCD outputs are the equivalent of numeric 0 and all Digit Select outputs are forced to the OFF condition. This remains until the Scan Input returns to logic 1. Built-in synchronization ensures that BCD data for the selected latch is valid prior to enabling the corresponding Digit Select Output.

The Digit Select Counter is a one-of-four counter, scanning from MSD (Most Significant Digit) to LSD (Least Significant Digit), enabling one quad latch output at a time, and presenting a logic 1 to the corresponding Digit Select output.

The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply.

TRANSFER LOGIC & TIMING

While the Transfer input is at logic 0,data in the decade counters is transferred to the static storage latches. This input may be left at 0 for a continuous transfer-and-display mode, or may be pulsed periodically to store only on command.

Termination of a transfer command occurs internally when the input is taken to a logic 1 and the next Count Input negative edge occurs. This allows asynchronous Count and Transfer operation since the transfer is terminated prior to incrementing the counters. This means that a Count Input negative edge must follow a Transfer command before a Reset is applied to prevent transfer of invalid data. An external Reset Command must be delayed at least one Count Input negative edge following a Transfer. External transfer should terminate at least 1 µs prior to this Count negative edge and Reset should occur no sooner than 1 µs following that edge.

RESET CONTROL

The decade counters are reset to 0,000 when the $\overline{\text{Reset Input}}$ is at logic 0. The $\overline{\text{Reset Input}}$ at logic 0 also forces the Scan to the MSD output. It maintains this condition as long as the logic 0 is present at the $\overline{\text{Reset Input}}$ and overrides all other associated inputs. As indicated previously, the decade counters should not be reset until a transfer has been terminated.

Since the $\overline{\text{Reset Input}}$ resets the Scan Counter to MSD the scan rate must be much faster than the reset rate to allow the lesser significant digits to be enabled. Therefore, F_{Scan}, must be much greater than four times F_{Reset}.

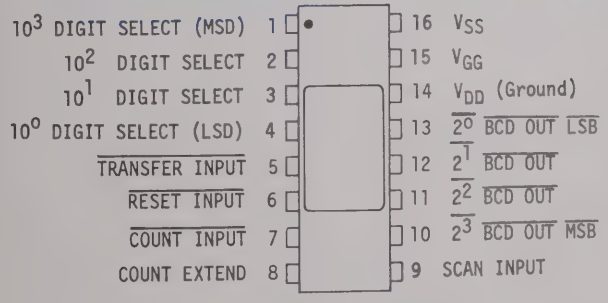
OUTPUTS

All output buffers on the MK 5007 P are push-pull. A negative power supply terminal, V_{GG}, is provided to increase the drive capabilities of these output buffers. Since the V_{GG} supply is connected only to these output buffers, it has no effect on any other device characteristics.

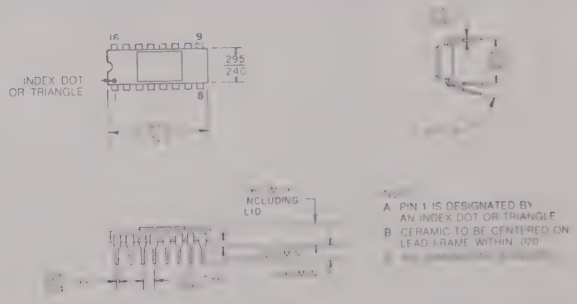
Output characteristics are covered in the MK 5002 Application Report which illustrates the effects of V_{GG} with current to be expected at various output voltages.

The outputs are designed to drive directly to the base of common-emitter transistors, so that output voltage is clamped or maintained at a potential where the MK 5007 P is able to sink or source its greatest amount of current.

PIN CONNECTIONS



PACKAGE (16-lead ceramic dual-in-line hermetic package)

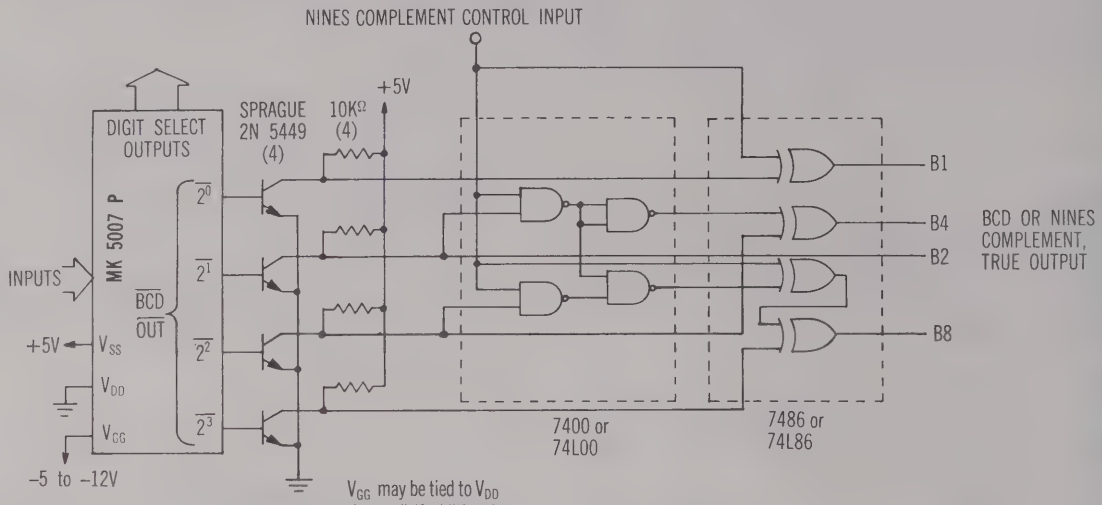

INDEX DOT OR TRIANGLE
INCLUDING LID
A PIN 1 IS DESIGNATED BY AN INDEX DOT OR TRIANGLE
B CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN .020

APPLICATION

A "down" count can be achieved by converting true BCD up-count to its nines complement, making the internal counter appear to be counting down.

The circuit shown will convert the negative-logic output of the MK 5007 P to a true BCD up-count when the Nines Complement Control is at Logic 0. With the Nines Complement Control at Logic 1, the output will be the nines complement of true BCD (see Truth Table).

Note that while the Nines Complement circuit permits the outputs to appear to be counting up or down, it will not function as a true up/down counter. However, in applications when the change from up-count to down-count occurs when the counter reaches all 9's (such as in DVM's), this circuit will function as an up/down counter.



V_{GG} may be tied to V_{DD} (ground) if additional resistors (150 KΩ) are connected from base-to-ground on the transistors (2N5449) shown at the $\overline{BCD}$ outputs of the MK 5007 P.

	MK 5007 P Output				NINES COMPLEMENT CIRCUIT OUTPUT							
					NINES COMPLEMENT CONTROL = 0				NINES COMPLEMENT CONTROL = 1			
	$\overline{MSB}$	$\overline{2^2}$	$\overline{2^1}$	$\overline{LSB}$	B^8	B^4	B^2	B^1	B^8	B^4	B^2	B^1
Digit 0	1	1	1	1	0	0	0	0	1	0	0	1
Digit 1	1	1	1	0	0	0	0	1	1	0	0	0
Digit 2	1	1	0	1	0	0	1	0	0	1	1	1
Digit 3	1	1	0	0	0	0	1	1	0	1	1	0
Digit 4	1	0	1	1	0	1	0	0	0	1	0	1
Digit 5	1	0	1	0	0	1	0	1	0	1	0	0
Digit 6	1	0	0	1	0	1	1	0	0	0	1	1
Digit 7	1	0	0	0	0	1	1	1	0	0	1	0
Digit 8	0	1	1	1	1	0	0	0	0	0	0	1
Digit 9	0	1	1	0	1	0	0	1	0	0	0	0

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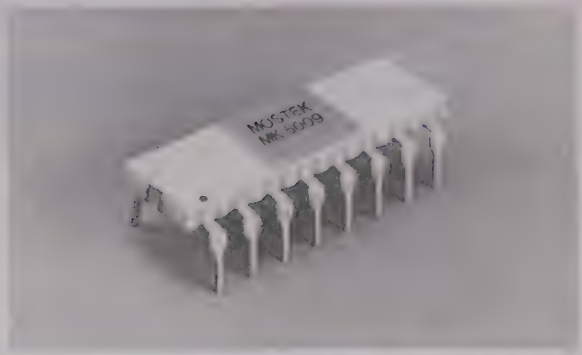
MK 5009 P

MOS Counter Time-Base Circuit

MOSTEK CORPORATION

DS-5009672-2 / AUG. 1972

- Ion-implanted for full TTL/DTL compatibility
- Internal clock operates from:
  - External signal
  - External RC network
  - External crystal
- Operates DC to above 1 MHz
- Binary-encoded for frequency selection



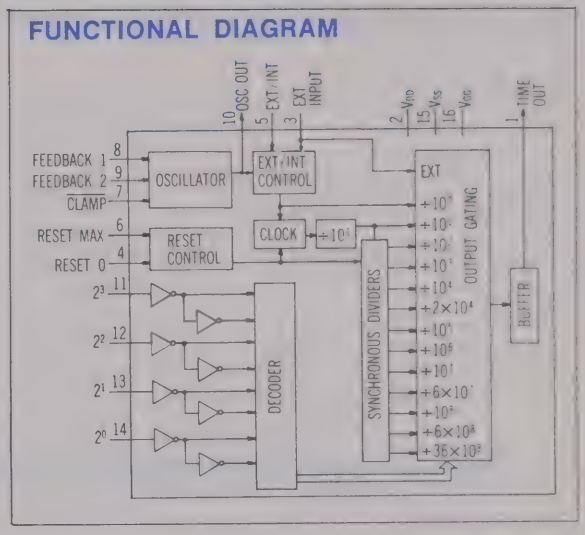
DESCRIPTION

The MK 5009 P is a highly versatile MOS oscillator and divider chain manufactured by Mostek using its depletion-load, ion-implantation process and P.-channel technology. The 16-pin DIP package provides frequency division ranges from 1 to 36×10^8. The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination; the internal oscillator with an external crystal; or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instruments, timers, and clocks.

With an input frequency of 1 MHz, the MK 5009 P provides the basic time periods necessary for most frequency measuring instruments, i.e., 1 μs through 100 seconds. One-minute, ten-minute, and one-hour periods are also available using a 1 MHz input. Using a 1/1.2 MHz input, the MK 5009 P can also provide a 50/60 Hz output for accurate generation of line frequencies in portable instruments or clocks.

The time-base output (TIME OUT) is a square wave, its frequency determined by the selected counter division, and by the oscillator frequency or external input. The falling edge of the output square wave should be used to control external gating circuitry.

FUNCTIONAL DIAGRAM



TIME OUT

ADDRESS INPUTS 2^3	2^2	2^1	2^0	WITHOUT RESET $R_{MAX}=0$ $R_O=0$	RESET Reset Max. $R_{MAX}=1$ $R_O=0$	RESET Reset Min. $R_{MAX}=0$ $R_O=1$	BYPASS MODES (see page 3) Mode 1 $R_{MAX}=V_{GG}$ $R_O=0$	Mode 2 $R_{MAX}=0$ $R_O=V_{GG}$	Mode 3 $R_{MAX}=V_{GG}$ $R_O=V_{GG}$
0	0	0	0	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$
0	0	0	1	$\div 10^1$			$\div 10^1$	$\div 10^1$	$\div 10^1$
0	0	1	0	$\div 10^2$	Resets	Resets	$\div 10^2$	$\div 10^2$	$\div 10^2$
0	0	1	1	$\div 10^3$			$\div 10^3$	$\div 10^3$	$\div 10^3$
0	1	0	0	$\div 10^4$	Counters	Counters	$\div 10^4$	$\div 10^4$	$\div 10^4$
0	1	0	1	$\div 10^5$			$\div 10^2$	$\div 10^5$	$\div 10^2$
0	1	1	0	$\div 10^6$	to their	to their	$\div 10^3$	$\div 10^6$	$\div 10^3$
0	1	1	1	$\div 10^7$			$\div 10^4$	$\div 10^7$	$\div 10^4$
1	0	0	0	$\div 10^8$	Highest	Lowest	$\div 10^5$	$\div 10^5$	$\div 10^2$
1	0	0	1	$\div 6\times10^7$			$\div 6\times10^4$	$\div 6\times10^4$	$\div 6\times10^1$
1	0	1	0	$\div 36\times10^8$	States	States	$\div 36\times10^5$	$\div 36\times10^5$	$\div 36\times10^2$
1	0	1	1	$\div 6\times10^8$			$\div 6\times10^5$	$\div 6\times10^5$	$\div 6\times10^2$
	*			—			—	—	—
1	1	1	0	$\div 2\times10^4$			$\div 2\times10^1$	$\div 2\times10^1$	$\div 2\times10^1$
1	1	1	1	Ext. In.	Ext. In.	Ext. In.	Ext. Int.	Ext. Int.	Ext. Int.

*Addresses 1100 and 1101 result in Logic 0 at the output regardless of the state of the Reset Max. and Reset Min. inputs.

Logic 1 = High = V_{SS}
Logic 0 = Low = V_{DD}

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MOSTEK CORPORATION ®

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} . . . . . + 0.3V to − 20V
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Storage Temperature Range (Ambient) . . . . . − 55°C to + 150°C

RECOMMENDED OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+ 4.5		+ 5.5	V	
V_{DD}	Supply Voltage	0.0		0.0	V	
V_{GG}	Supply Voltage	− 9.6		− 14.4	V	
f_{XTAL}	Crystal Frequency	0.1		2.0	MHz	
f_{RC}	RC Frequency	DC		200	kHz	
f_{EXT}	External Frequency	DC		2.0	MHz	
t_{PL}	Logic 0 Pulse Width, $\overline{CLAMP}$	—				Note 5
	Ext. Input	200			nsec	
t_{PH}	Logic 1 Pulse Width, Ext. Input	200			nsec	
	Reset Max	10.0			μsec	
	Reset 0	10.0			μsec	
R	Feedback Resistance	.01		2.5	MΩ	Fig. 1
V_{IL}	Input Voltage, Logic 0, Reset Inputs	0.0		0.8	V	
	Reset (Bypass Mode)	V_{GG}		V_{GG} + 1.0	V	Note 2
	All Other Logic Inputs			0.8	V	
V_{IH}	Input Voltage, Logic 1, All Logic Inputs	V_{SS}-1.0	V_{SS}	V_{SS} + 0.3	V	

ELECTRICAL CHARACTERISTICS

((V_{SS} = +5V ±10%; V_{DD} = 0 V; V_{GG} = −12.0 V ±20%; 0° C ≤ T_A ≤ 70°C)

	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
I_{SS}	Supply Current, V_{SS}		6.0	11.0	mA	Note 1
I_{GG}	Supply Current, V_{GG}		6.0	11.0	mA	
I_{IL}	Input Current, Logic 0			− 1.6	mA	Note 2; V_I = 0.4V
V_{OL}	Output Voltage, Logic 0			0.4	V	I_{OL} = 1.6mA*
V_{OH}	Output Voltage, Logic 1	2.4			V	I_{OH} = −40μA*
f_{STA}	Frequency Stability w/ Volt. Change, RC Mode		± 3.0		%/V	Note 3
	/ Temp. Change, RC Mode		− 0.2		%/°C	
	Crystal Mode		—			Note 4
$t_{e\ e}$	Jitter, Edge-to-Edge Variation		<15		nsec	Temp. & Supply Voltage Constant

*Typical values at V_{SS} = +5V, V_{DD} = 0V, V_{GG} = −12V, and T_A = 25°C

1. Logic inputs at V_{SS}, output open circuited. Each logic input (see Note 2) contributes an additional 1.6 mA (max.) to I_{SS} when at logic 0.
2. Logic Inputs are: Reset Max; Reset 0; Address Inputs; Ext. Input; Ext/Int Select; and $\overline{Clamp}$.
3. Frequency variations due to power supply changes only.
4. Crystal mode stability is dependent upon crystal.
5. Minimum logic 0 time at clamp input is 50% of oscillator period.

*V_{OH}, V_{OL} apply only to Time Out.

DESCRIPTION OF OPERATION

The MK 5009 P consists basically of a series of counters, selectable via an internal multiplexer. The $\div 10^1$ counter output is used to generate an internal clock signal for the 10^2 through 36×10^8 counter stages, which are fully synchronous with each other.

OSCILLATOR CONTROLS

Operation in the RC oscillator mode is achieved as shown in Figure 1. Frequency, f, is approximately 0.8/RC. The clamp circuit can be used in the RC mode to provide one-shot or accurate start-up operations. When Clamp goes to a logic 0, the internal circuitry is held at a reference level so that upon release of the Clamp (return to logic 1), the oscillator's first cycle will be a full cycle.

The crystal oscillator mode is shown in Figure 2. Values for the resistors are chosen to bias the internal circuitry for optimum performance. The two capacitors are chosen to provide the loading capacitance (C_L) specified for the selected crystal. It is recommended that C1 = C2 = 2 C_L.

RESET/BYPASS CONTROLS

The MK 5009 P provides two different reset conditions. A positive-going pulse of 10 μs or longer on Reset 0 will reset counters to their lowest state, while a positive-going pulse at Reset Max will reset counters to their highest state. The Reset Max control enables the user to set up the counters to provide a falling edge at the next oscillator cycle or negative-going external input, regardless of which divider chain is selected.

In addition, taking one or both Reset Inputs to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes (see table on page 1).

EXTERNAL/INTERNAL FREQUENCY SOURCE

When using an external signal source to operate the MK 5009 P, that signal should be applied at the External Input (Pin 3), and the External/Input Select (Pin 5) should be brought to logic 1.

For operation with an internal signal, the External/Internal Select should be at logic 0.

OSCILLATOR OUTPUT

The oscillator output, provided at Pin 10, is not a true logic output, but may be used to drive a high impedance device such as a junction FET or other MOS circuitry.

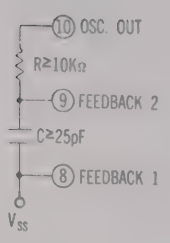


FIG. 1

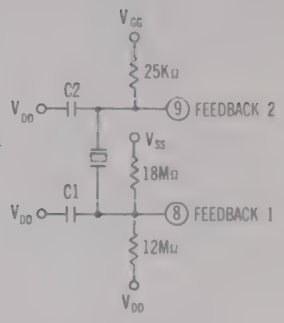
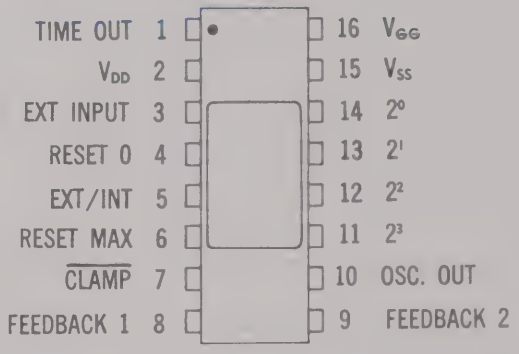
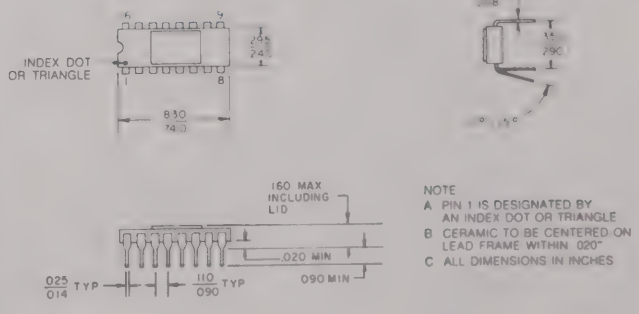


FIG. 2

PIN CONNECTIONS



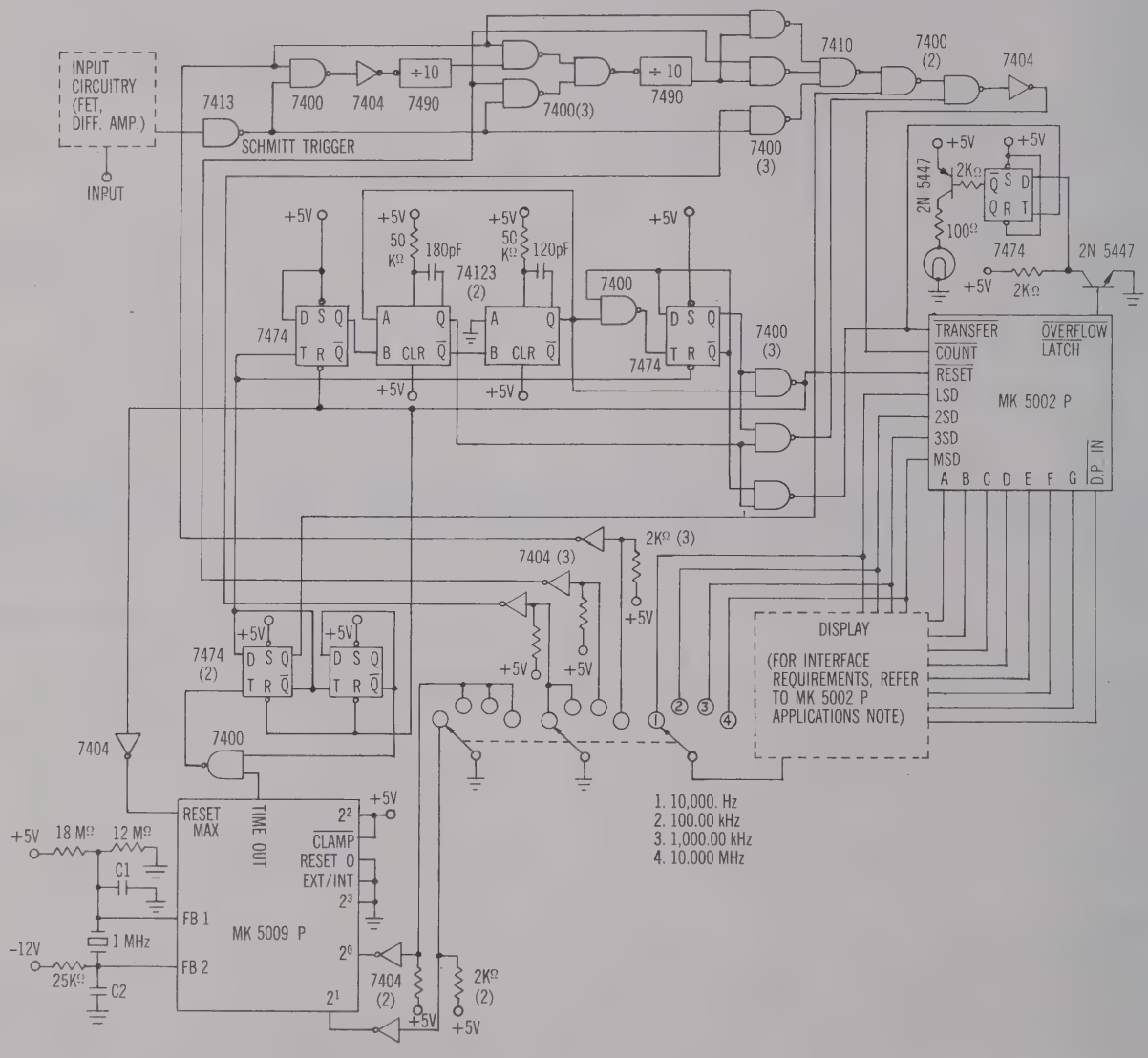
PACKAGE (16-lead ceramic dual-in-line hermetic package)


INDEX DOT OR TRIANGLE
.160 MAX INCLUDING LID
.020 MIN
.090 MIN
.025/.014 TYP
.110/.090 TYP
NOTE
A PIN 1 IS DESIGNATED BY AN INDEX DOT OR TRIANGLE
B CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN .020"
C ALL DIMENSIONS IN INCHES

APPLICATION — 10 MHz Frequency Counter

The circuit shown below is a frequency counter capable of counting input rates up to 10 MHz, selected in four ranges. The MK 5009 P provides the time base intervals while the Mostek MK 5002 P counter circuit provides counting, storage, and display functions. Two decades of prescaling using TTL are employed. TTL one-shots provide proper timing for the 5002.

To replace the functions of the MK 5009 P, an active device and Schmitt trigger for the crystal oscillator would be needed, plus six 7490's to achieve the correct time out. Replacing the functions of the MK 5002 would require four 7490's, four 7475's, and four BCD-to-seven-segment decoders.



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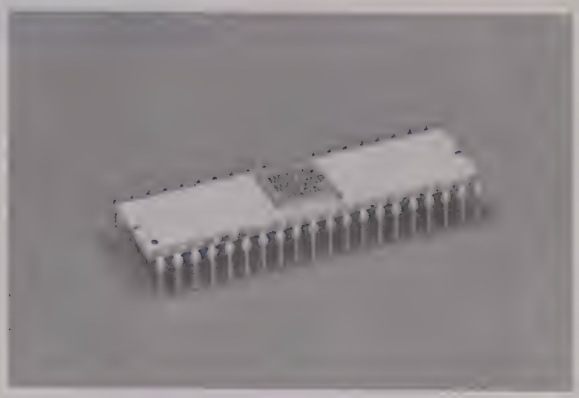
MOS 10-Digit Calculator

MOSTEK CORPORATION

DS-50101171-3 / AUG. 1972

FEATURES

- ☐ 10 digits
- ☐ Four operations (+, ×, —, ÷)
- ☐ Floating-point input and fixed-point resultant selectable to 0, 2, 3 or 4 places
- ☐ Chain calculations
- ☐ "Credit" balance
- ☐ Seven- or eight-segment outputs
- ☐ Decoded digit select provided
- ☐ Leading zero blanking
- ☐ Overflow indication



DESCRIPTION

Calculations, including addition, subtraction, multiplication and division, with resultant display of up to 10 digits and decimal point, are provided with Mostek's MK 5010 P. Mostek's ion implantation is employed with MOS P-channel technology to lower threshold voltages and reduce power requirements. All inputs are internally protected against static charge accumulation.

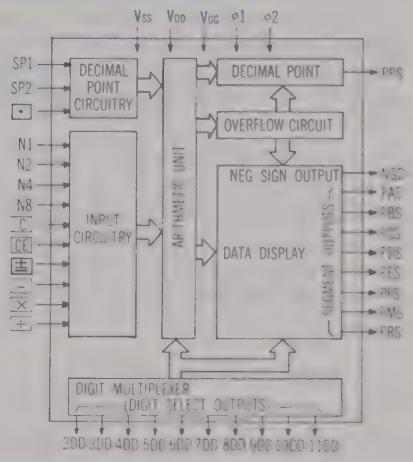
The MK 5010 P requires only simple, external binary encoding of the numeric keys (see Table IA for coding) for inputs at N_1, N_2, N_4 and N_8. These inputs are sensed for their logic state; entry is made with logic 1 at any input, and previous entries are shifted to the left. With all inputs at logic 0, completion of entry occurs.

The numeric entry, or the resulting calculation, is displayed on a scan or strobed basis. A one-of-ten output at the Digit Select outputs enables the appropriate (selected) display digit. 11DD corresponds to the Most Significant Digit (MSD) while 2DD corresponds to the Least Significant Digit (LSD).) As outputs are scanned from LSD to MSD, the appropriate data for each selected digit appears at the segment outputs. Segment data is ensured to be valid prior to enabling the Digit Select output.

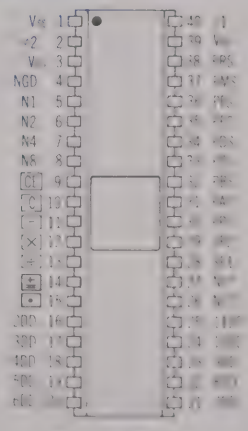
By inhibiting the appropriate Digit Select outputs, the MK 5010 P provides blanking of leading zeros; meaningless zeros to the left of the decimal point, except the 10^0 digit, are not displayed. All digits are blanked during calculation time (t_{Cal}).

Decimal point location may be selected to provide results in units only (0 places); in hundredths (2 places); in thousandths (3 places); or ten-thousandths (4 places). This selection is made at inputs SP1 and SP2 (see Table 1B for coding). Numeric entry may also be carried as far as the selected decimal point placement; further entry past this selected decimal point placement is disregarded.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



*NC = NO CONNECTION
DO NOT USE AS TIE POINT

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OPERATING CHARACTERISTICS

I. CODING (See Specifications for logic level definitions).

TABLE IA: CODING FOR NUMERIC INPUTS

Desired Numeric Input	Logic Inputs N_8	N_4	N_2	N_1
0	1	0	1	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

TABLE IB: CODING FOR DECIMAL POINT PLACEMENT

Desired Decimal Location	Logic Input SP 1	SP 2
0	0	0
2	1	0
3	0	1
4	1	1

II. OVERFLOW

Overflow occurs when a numeric entry exceeds 10 digits, or a resultant calculation exceeds 10 digits, or any entry exceeds 10 digits when carried to the selected number of decimal places. When overflow occurs, the display becomes all 0's, with the decimal point output (PPS) in a static logic 1 condition so the displayed reading becomes 0 0 0 0 0.0.0.0.0.0. . (Decimal Point on Digit 6 [7DD] is not normally used, but may be connected to the Decimal Point output, as shown on the schematic, for clearer indication of overflow. Decimal Points for digits 7 to 10 [DD8 to DD11] should never be connected.)

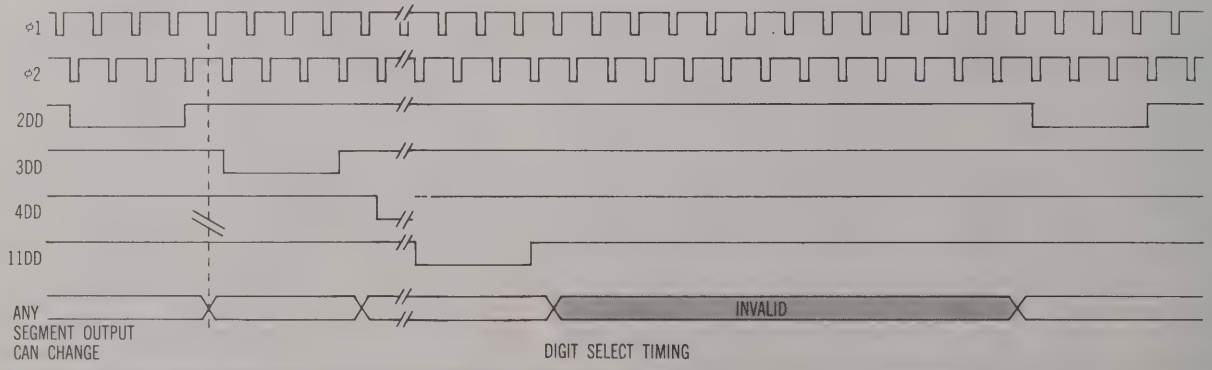
III. CLEAR AND CLEAR ENTRY

The Clear Input provides a complete clearing of *all* entries and resultant calculations. Clear Entry provides clearing of all numeric entries following the last function command, but does not clear previous entries stored in the register that are awaiting calculation.

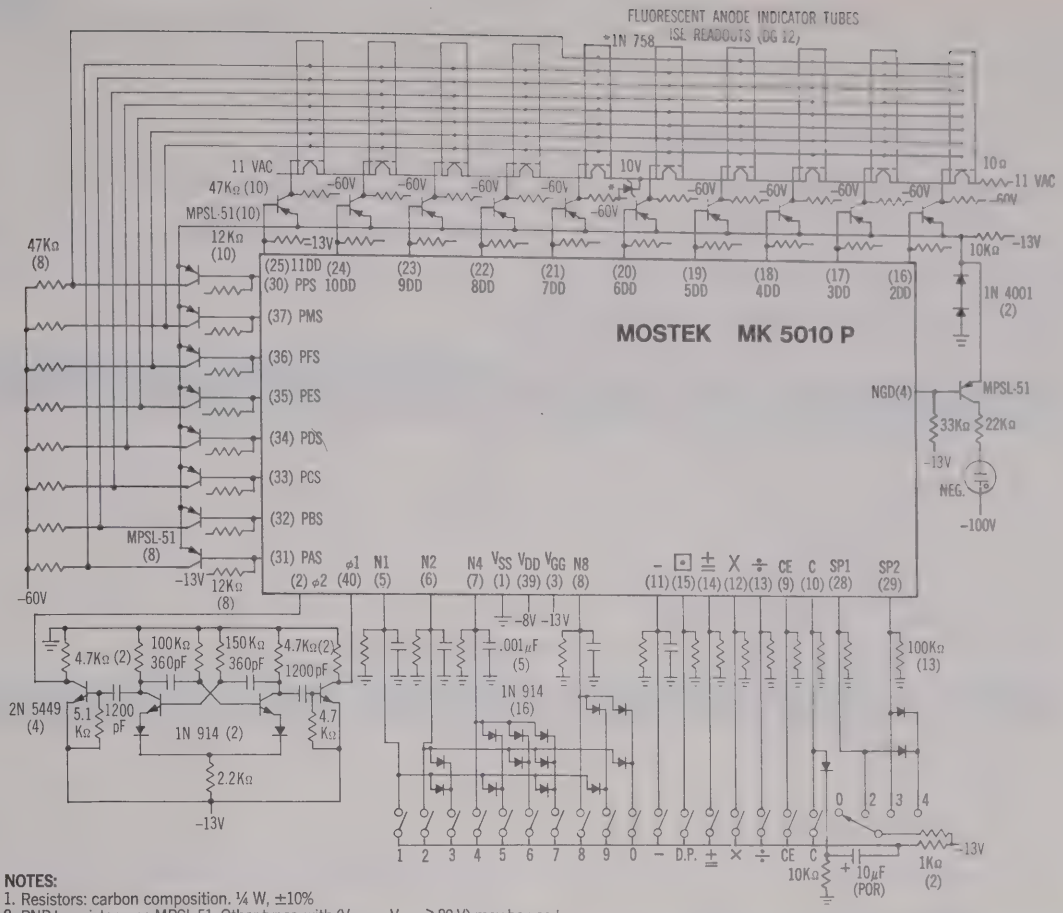
Either Clear or Clear Entry at logic 1 provides a display of all 8's for a convenient lamp test. Completion of Clear or Clear Entry produces a numeric zero display.

IV. MOS OUTPUTS

The MOS outputs are open drain buffers which are turned ON to V_{SS} for a logic 0 output and represent an open circuit when turned off (logic 1). Timing of the Digit Select outputs, relative to $\phi 2$ clocking and to each other, is as follows. Only *one* of the Digit Select outputs is selected (logic 1) at any one time. As noted in the timing, there is an inter-digit blanking period, so that any one digit is actually selected for only 75% of the total time allotted to that digit. There is also a blanking period between the MSD (11DD) selected time and the return to the LSD (2DD) selected time, equal to three total digit times. The display time for any one digit is then approximately 1/17 or 6% of the total scan time. This percentage may then be used in determining peak currents or voltages required by the display elements.



DIGIT SELECT TIMING

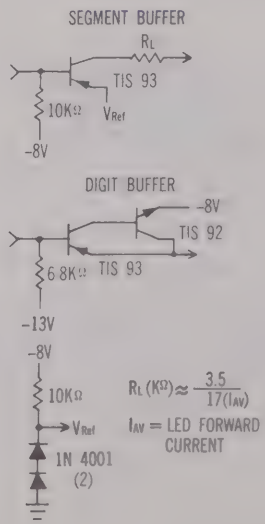


NOTES:
1. Resistors: carbon composition. ¼ W, ±10%
2. PNP transistors are MPSL 51. Other types with ($V_{BCO} = V_{CEO} \geq 80$ V) may be used. (Examples: 2N 4888, 2N 5400.)

SAMPLE PROBLEM $\dfrac{(53.6 + 12.32 - 96)\,(2.2)}{5} = 13.23$ (DP = 2)

Key Input Sequence	Display (Output)										
C								0.	0	0	
5										5	
3									5	3	
·									5	3.	
6								5	3.	6	
±							5	3.	6	0	
1										1	
2									1	2	
·									1	2.	
3								1	2.	3	
2							1	2.	3	2	
±							6	5.	9	2	
9										9	
6									9	6	
−							3	0.	0	8	Neg
×							3	0.	0	8	Neg
2										2	
·										2.	
2									2.	2	
÷							6	6.	1	7	Neg
5										5	
±							1	3.	2	3	Neg

INTERFACING COMMON-CATHODE LED's.



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MK 5012 P

MOS 12-Digit Calculator

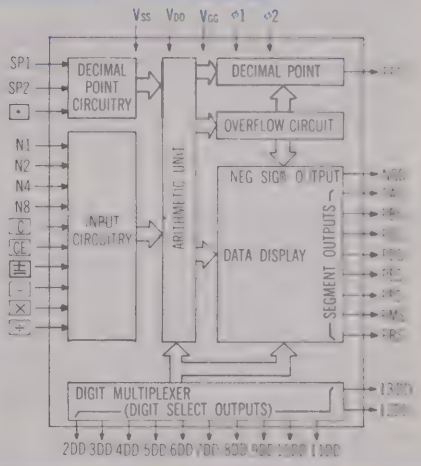
MOSTEK

DS-5012172-3/MAY 1973

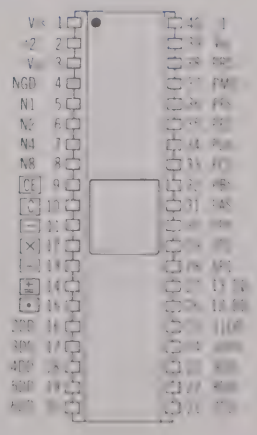
FEATURES

- ☐ 12 digits
- ☐ Four operations (+,×,−,÷)
- ☐ Floating-point input and fixed-point resultant selectable to 0, 2, 3 or 4 places
- ☐ Chain calculations
- ☐ "Credit" balance
- ☐ Seven- or eight-segment outputs
- ☐ Decoded digit select provided
- ☐ Leading zero blanking
- ☐ Overflow indication

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



Calculations, including addition, subtraction, multiplication and division, with resultant display of up to 12 digits and decimal point, are provided with Mostek's MK 5012 P. Mostek's ion implantation is employed with MOS P-channel technology to lower threshold voltages and reduce power requirements. All inputs are internally protected against static charge accumulation.

The MK 5012 P requires only simple, external binary encoding of the numeric keys (see Table IA for coding) for inputs at N_1, N_2, N_4 and N_8. These inputs are sensed for their logic state; entry is made with logic 1 at any input, and previous entries are shifted to the left. With all inputs at logic 0, completion of entry occurs.

The numeric entry, or the resulting calculation, is displayed on a scan or strobed basis. A one-of-twelve output at the Digit Select outputs enables the appropriate (selected) display digit. 13DD corresponds to the Most Significant Digit (MSD) while 2DD corresponds to the Least Significant Digit (LSD). As outputs are scanned from LSD to MSD, the appropriate data for each selected digit appears at the segment outputs. Segment data is ensured to be valid prior to enabling the Digit Select output.

By inhibiting the appropriate Digit Select outputs, the MK 5012 P provides blanking of leading zeroes; meaningless zeroes to the left of the decimal point, except the 10^0 digit, are not displayed. All digits are blanked during calculation time (t_{Cal}).

Decimal point location may be selected to provide results in units only (0 places); in hundredths (2 places); in thousandths (3 places); or ten-thousandths (4 places). This selection is made at inputs SP1 and SP2 (see Table 1B for coding). Numeric entry may also be carried as far as the selected decimal point placement; further entry past this selected decimal point placement is disregarded.

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OPERATING CHARACTERISTICS

I. CODING (See Specifications for logic level definitions).

TABLE IA: CODING FOR NUMERIC INPUTS

Desired Numeric Input	Logic Inputs N_8	N_4	N_2	N_1
0	1	0	1	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

TABLE IB: CODING FOR DECIMAL POINT PLACEMENT

Desired Decimal Location	Logic Input SP 1	SP 2
0	0	0
2	1	0
3	0	1
4	1	1

II. OVERFLOW

Overflow occurs when any numeric entry or resultant addition or multiplication exceeds 12 digits when carried to the selected number of decimal points. A multiplicand exceeding 11 digits results in overflow following calculation with any multiplier. In division calculations, the number of digits in the divisor usually cannot exceed 10, while the quotient and dividend are limited to 11 digits.

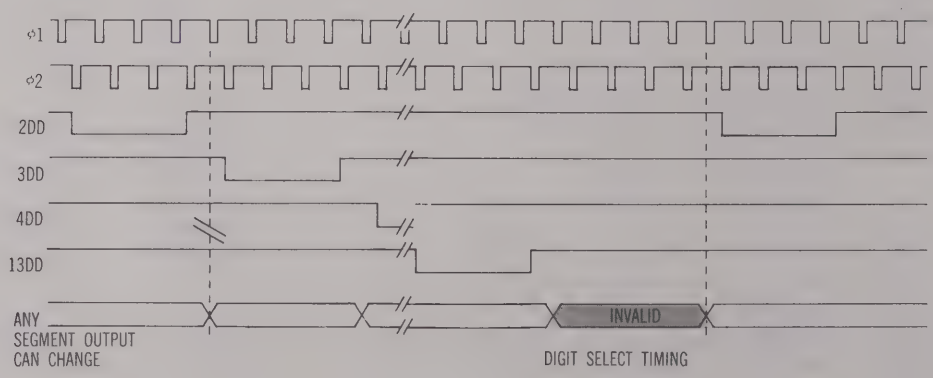
When overflow occurs, the display becomes all 0's, with the decimal point output (PPS) in a static logic 1 condition so the displayed reading becomes 0 0 0 0 0 0 0.0.0.0.0.0. . (Decimal Point on on Digit 6 (7DD) not normally used, but may be connected to the Decimal Point output, as shown on the schematic, for clearer indication of overflow. Decimal Points for digits 7 to 12 (DD8 to DD13) should never be connected.)

III. CLEAR AND CLEAR ENTRY

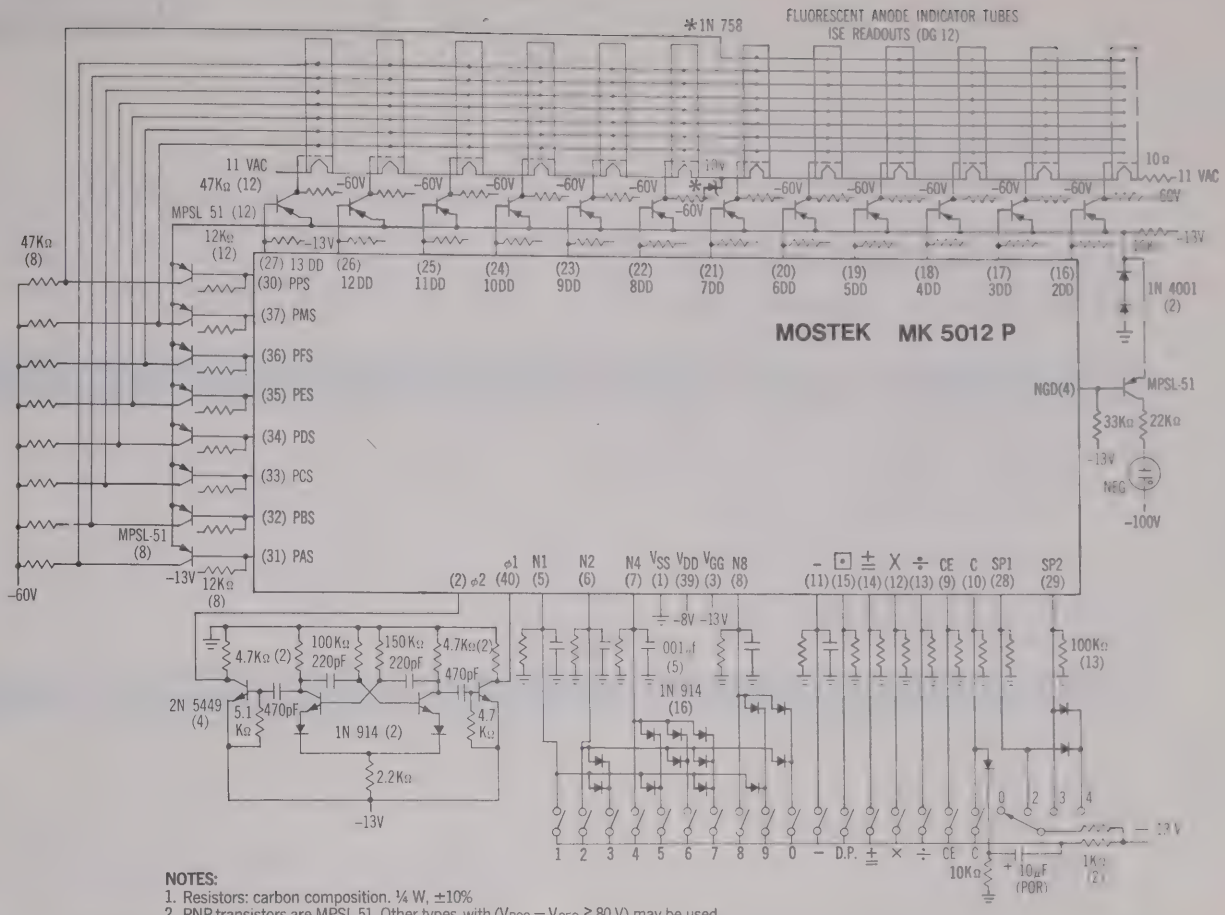
The Clear Input provides a complete clearing of *all* entries and resultant calculations. Clear Entry provides clearing of all numeric entries following the last function command, but does not clear previous entries stored in the register that are awaiting calculation. Either Clear or Clear Entry at logic 1 provides a display of all segments for a convenient lamp test. Completion of Clear or Clear Entry produces a numeric zero display.

IV. MOS OUTPUTS

The MOS outputs are open drain buffers which are turned ON to V_{SS} for a logic 0 output and represent an open circuit when turned off (logic 1). Timing of the Digit Select outputs, relative to $\phi 2$ clocking and to each other, is as follows. Only *one* of the Digit Select outputs is selected (logic 1) at any one time. As noted in the timing, there is an inter-digit blanking period, so that any one digit is actually selected for only 75% of the total time allotted to that digit. There is also a blanking period between the MSD (13DD) selected time and the return to the LSD (2DD) selected time, equal to one digit time. The display time for any one digit is then approximately 1/17 or 6% of the total scan time. This percentage may then be used in determining peak currents or voltages required by the display elements.



DIGIT SELECT TIMING

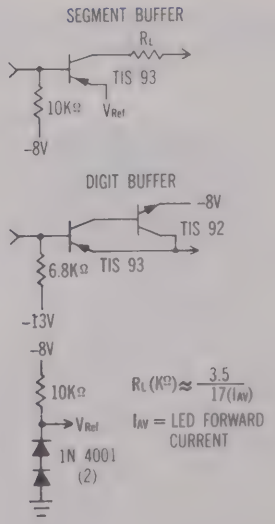


NOTES:
1. Resistors: carbon composition. ¼ W, ±10%
2. PNP transistors are MPSL 51. Other types with ($V_{BCO} = V_{CEO} \geq 80$ V) may be used. (Examples: 2N 4888, 2N 5400.)

SAMPLE PROBLEM $\frac{(53.6 + 12.32 - 96)(2.2)}{5} = 13.23$ (DP = 2)

Key Input Sequence	Display (Output)	
C	0.	0
5		5
3		53
.		53.
6	5	3.6
±	5	3.60
1		1
2		12
.		12.
3	1	2.3
2	1	2.32
±	6	5.92
9		9
6		96
-	3	0.08 Neg
X	3	0.08 Neg
2		2
.		2.
2		2.2
÷	6	6.17 Neg
5		5
±	1	3.23 Neg

INTERFACING COMMON-CATHODE LED'S



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PRODUCT DESCRIPTION

MK 5013 P
MK 5014 P

PD-5013172-2/JAN. 1972

MOS 12-Digit Memory Calculator

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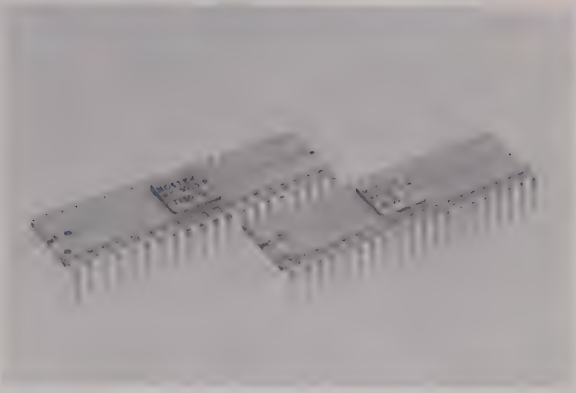
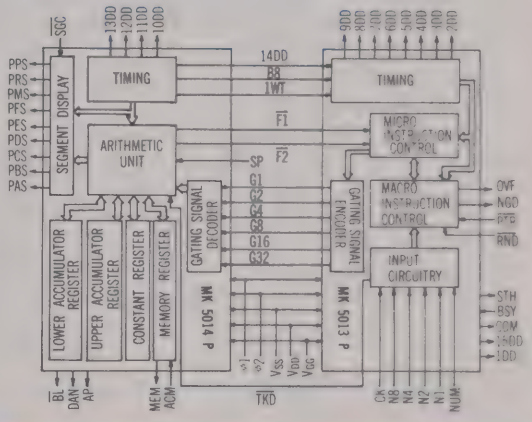


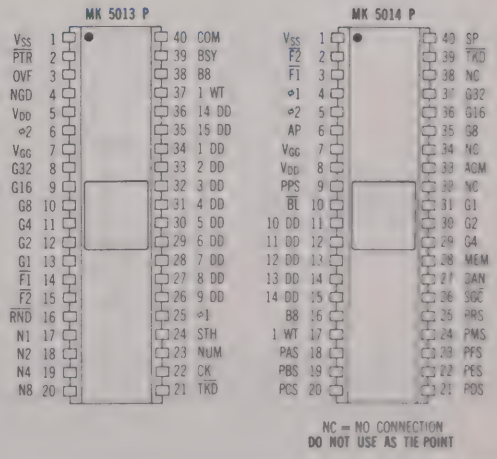
FEATURES

- 12-digit display with memory capability
- Four operations (+, −, ×, ÷)
- Automatic constant
- Floating decimal on entry and intermediate multiplication or division
- Fixed-decimal on total results selectable to *any* position in the display
- Memory overflow protection
- Overflow indicator
- Memory-in-use indicator
- Negative sign indicator for true credit balance
- Chain calculations
- Selectable truncate or 5/4 round-off
- Register exchange function
- Leading-zero blanking
- Print-out capability with the MK 5015 P
- Power-on clear capability
- 00-entry key

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



DESCRIPTION

The MK 5013/5014 P employs three working registers and one memory register to provide a four-function (+, −, ×, ÷), 12-digit display calculator. A third circuit, MK 5015 P, may be used with these two circuits to interface to a printer.

The MK 5013/5014 P calculator pair are P-channel MOS/LSI circuits employing Mostek's ion-implantation processing to lower threshold voltages and reduce power dissipation. All inputs are internally protected against static charge accumulation.

Key debounce is provided on-chip while simple encoding allows convenient use of available keyboards. Digit Select outputs (one-of-twelve) provide the enabling strobes to scan the display. As outputs are scanned from LSD (Least Significant Digit) to MSD (Most Significant Digit), the appropriate data for each selected digit appears at the segment outputs. Leading zero blanking is accomplished by inhibiting the segment outputs during the appropriate digit times.

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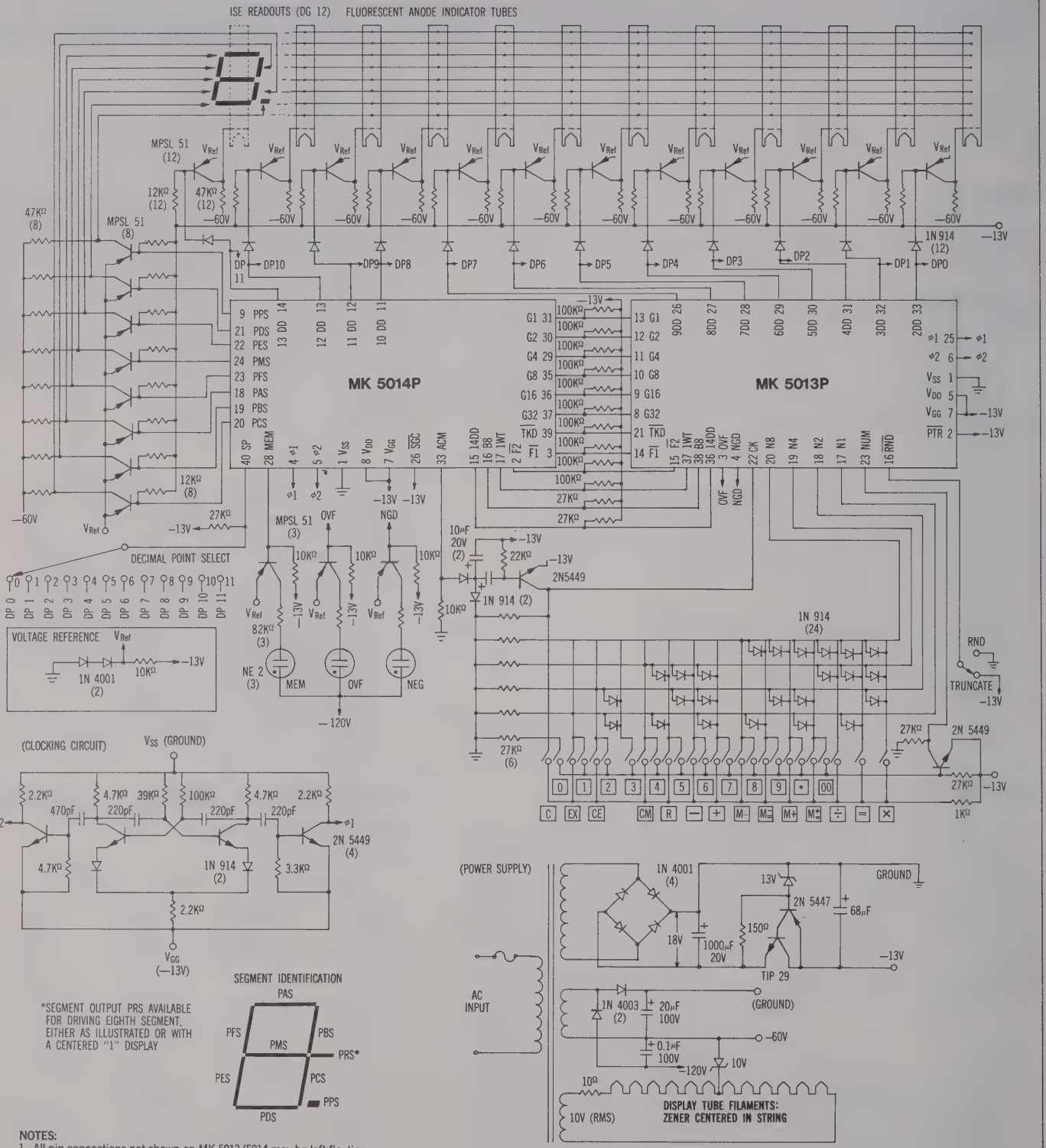
SCHEMATIC



NOTES:
1. All pin connections not shown on MK 5013/5014 may be left floating.
2. Resistors: carbon composition. ¼ W, ±10%
3. PNP transistors are MPSL 51. Other types with ($V_{BCO} = V_{CEO} \geq 80$ V) may be used. (Examples: 2N 4888, 2N 5400.)

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PRODUCT DESCRIPTION MK 5013 P MK 5014 P

PD-5013172-2/JAN. 1972

MOS 12-Digit Memory Calculator

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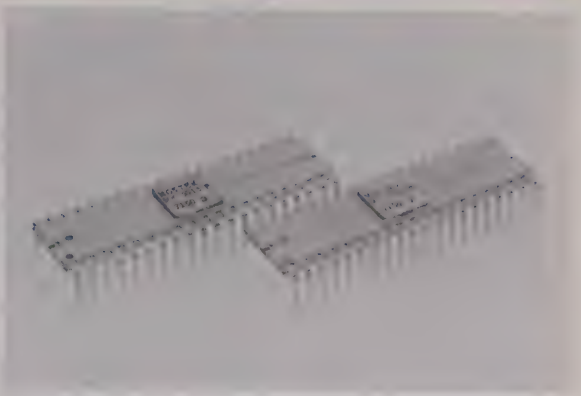
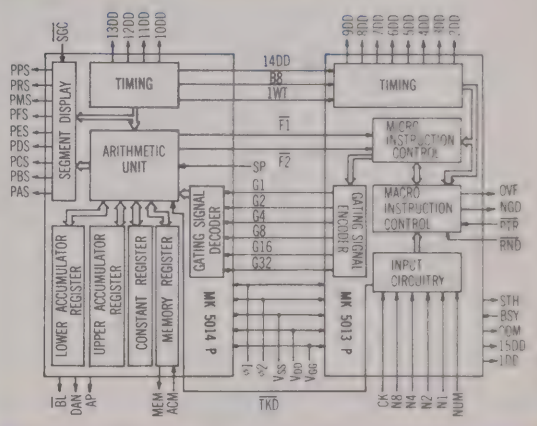


FEATURES

- 12-digit display with memory capability
- Four operations (+, −, ×, ÷)
- Automatic constant
- Floating decimal on entry and intermediate multiplication or division
- Fixed-decimal on total results selectable to *any* position in the display
- Memory overflow protection
- Overflow indicator
- Memory-in-use indicator
- Negative sign indicator for true credit balance
- Chain calculations
- Selectable truncate or 5/4 round-off
- Register exchange function
- Leading-zero blanking
- Print-out capability with the MK 5015 P
- Power-on clear capability
- 00-entry key

FUNCTIONAL DIAGRAM



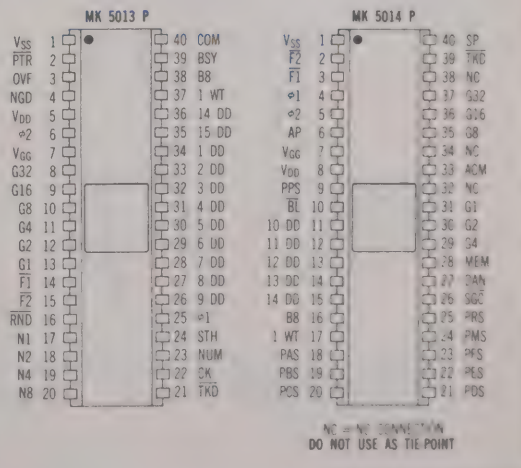
DESCRIPTION

The MK 5013/5014 P employs three working registers and one memory register to provide a four-function (+, −, ×, ÷), 12-digit display calculator. A third circuit, MK 5015 P, may be used with these two circuits to interface to a printer.

The MK 5013/5014 P calculator pair are P-channel MOS/LSI circuits employing Mostek's ion-implantation processing to lower threshold voltages and reduce power dissipation. All inputs are internally protected against static charge accumulation.

Key debounce is provided on-chip while simple encoding allows convenient use of available keyboards. Digit Select outputs (one-of-twelve) provide the enabling strobes to scan the display. As outputs are scanned from LSD (Least Significant Digit) to MSD (Most Significant Digit), the appropriate data for each selected digit appears at the segment outputs. Leading zero blanking is accomplished by inhibiting the segment outputs during the appropriate digit times.

PIN CONNECTIONS



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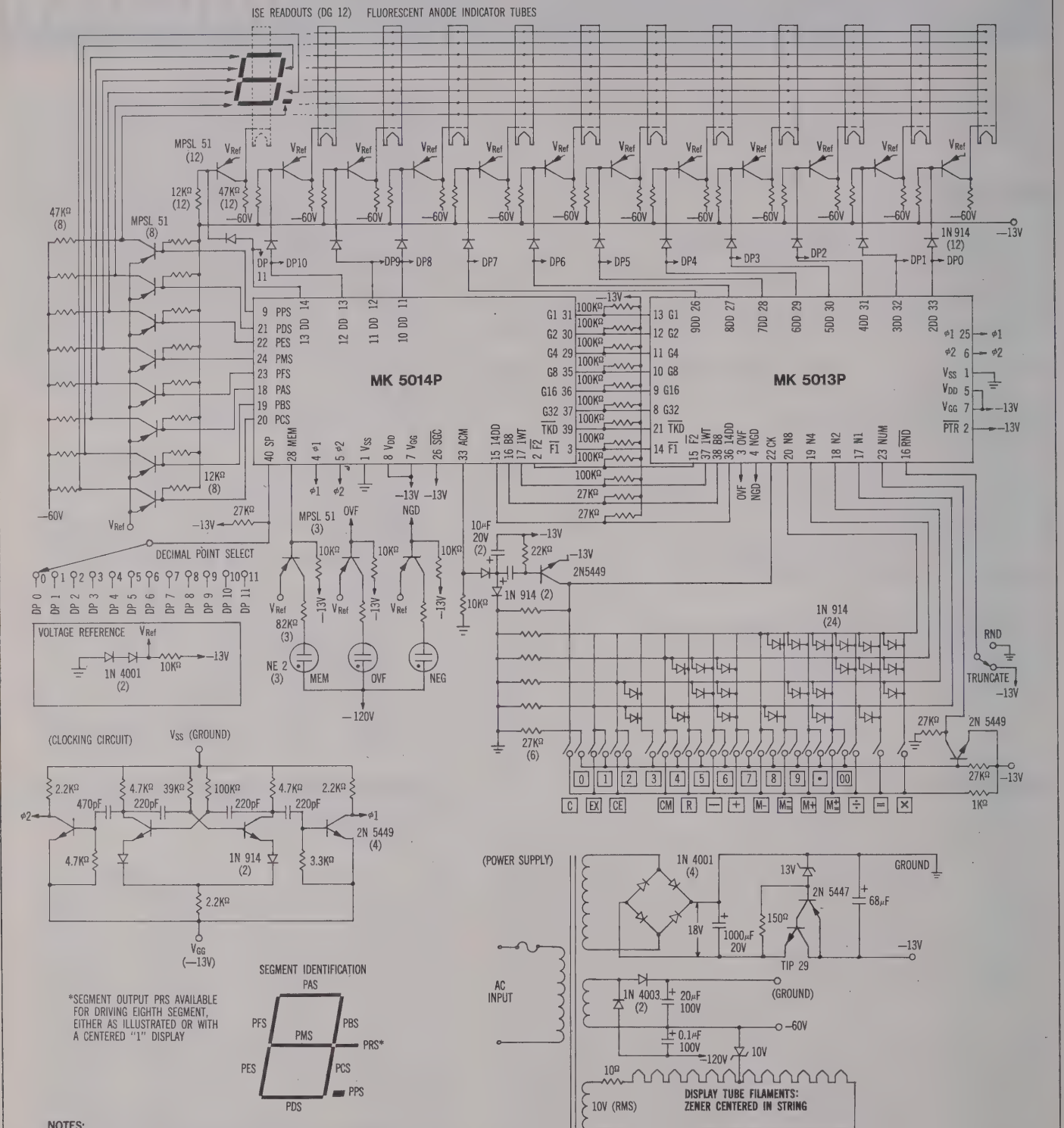
SCHEMATIC



*SEGMENT OUTPUT PRS AVAILABLE FOR DRIVING EIGHTH SEGMENT, EITHER AS ILLUSTRATED OR WITH A CENTERED "1" DISPLAY

NOTES:

1. All pin connections not shown on MK 5013/5014 may be left floating.
2. Resistors: carbon composition. ¼ W, ±10%
3. PNP transistors are MPSL 51. Other types with ($V_{BCO} = V_{CEO} \geq 80$ V) may be used. (Examples: 2N 4888, 2N 5400.)

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MK 5017 P

MOS Clock Circuit

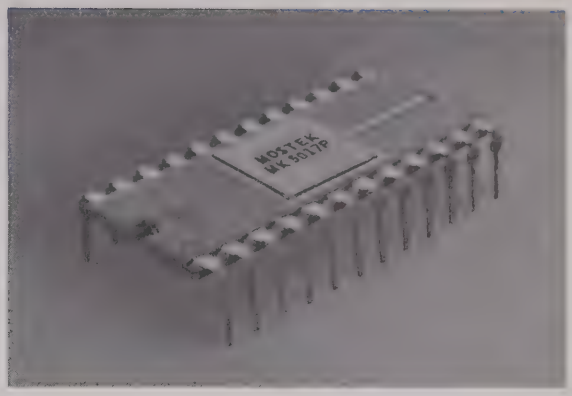
MOSTEK

DS-5017373-1 / MARCH 1973

FEATURES

- 6-digit display
- 12/24 hour operation and display
- 50/60 Hz input
- Single power supply operation
- Easy to set
- Standard products available

Alarm Clock	MK 5017 P AA
Clock Radio Clock	MK 5017 P AN
Calendar Clock	MK 5017 P BB



DESCRIPTION

The MK 5017 P is a versatile MOS/LSI clock circuit manufactured by MOSTEK using its depletion-load, ion-implantation process and P Channel technology. Intended for a wide range of timing applications, all of these clock circuits may be used with either four or six digit displays. These clock circuits feature full 12 and 24 hour timekeeping operation. Either a 12 or 24 hour display may be selected without disturbing counter contents since only the display format circuitry is affected. Operation from either a 50 Hz or 60 Hz input frequency may be selected. Another MOSTEK circuit (the MK 5009 P) is available to provide a 50 Hz signal from a 1 MHz crystal, where line frequency control is unavailable or inaccurate. A 50/60 Hz oscillator on the chip provides a temporary time base during momentary line frequency interruptions so that timekeeping can continue if a backup battery is provided to maintain V_{DD}.

Only a single power supply is required for operation. All segments are turned on (pulled toward V_{SS}) causing an all "8's" display as a power failure indication when V_{DD} is below the operating range.

Data is multiplexed out of the clock in the form of six sequential seven-segment decoded digits. The segment coding is shown in figure 1.

A scanning technique is employed to sense control switch closures in order to minimize input pin connections. Using this method only two pins, KA and KB, are required to sense up to 12 control switch closures.

SEGMENT IDENTIFICATION

FIGURE 1

SEGMENT CODING

	SA	SB	SC	SD	SE	SF	SG
0	1	1	1	1	1	1	
1		1	1				
2	1	1		1	1		1
3	1	1	1	1			1
4		1	1			1	1
5	1		1	1		1	1
6	1		1	1	1	1	1
7	1	1	1				
8	1	1	1	1	1	1	1
9	1	1	1	1		1	1

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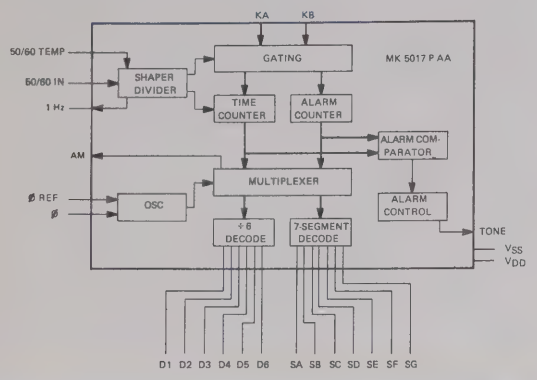
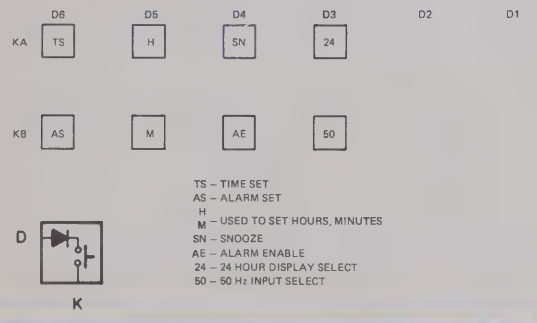
MOSTEK **MK 5017 AA**

Digital Alarm Clock

FUNCTIONAL DIAGRAM

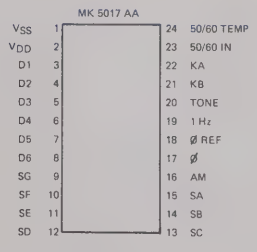


INPUT MATRIX



TS – TIME SET
AS – ALARM SET
H
M – USED TO SET HOURS, MINUTES
SN – SNOOZE
AE – ALARM ENABLE
24 – 24 HOUR DISPLAY SELECT
50 – 50 Hz INPUT SELECT

MOS/LSI DIGITAL ALARM CLOCK



FEATURES

- Alarm with 24 hour operation
- Alarm tone generated on-chip
- AM/PM indication
- Snooze
- 1 Hz output

DESCRIPTION

Time may be set in the Run mode while the clock circuit is counting or the clock may be set in the Time Set mode while the counters are stopped. Contents of the time counters is displayed in both the Time Set and Run modes. The clock is in the Time Set mode when the (TS) switch located at the intersection of the KA and D6 lines in the input matrix is closed. In the Time Set mode the time counters are stopped and the seconds and tens of seconds digits are reset to zero.

The clock is in the Run mode when both the (TS) and the Alarm Set (AS) switches are open. In the Run mode, counters less significant than the one being set continue counting.

Switches (M) and (H) in the input matrix are closed to cause individual digits to be incremented. The (M) switch causes the minutes digit to be incremented. The (H) switch causes the hours digits to be incremented. Closing both the (H) and (M) switches simultaneously causes the tens of minutes digit to be incremented. Incrementing of a selected digit occurs at a 2 Hz rate and with the exception of the tens of hours digit, digits more significent than the one being set will not increment.

In order to accurately set the time to the nearest second the clock should be placed in the Time Set mode. After setting the time ahead, the clock should then be returned to the Run mode at the proper time in order to start the clock.

The clock must be placed in the Alarm Set mode by closing the (AS) switch to set the alarm. In the Alarm Set mode the time counters continue timekeeping and the contents of the alarm counter is displayed. The alarm may be set to the nearest minute by manipulating the (H) and (M) switches in the same manner as when setting the time.

Both the time counters and the alarm counters have an AM/PM indication which allows the time and the alarm to be set on a 24 hour basis, rather than a 12 hour basis.

The Tone output occurs when coincidence between the alarm counters and the time counters is detected internally, if the alarm is enabled. The Tone output signal is a train of positive going pulses whose nominal frequency is equal to the frequency of the scan oscillator divided by 140 and modulated at a 1 Hz

rate. For a scan rate oscillator frequency of 100 KHz the Tone output frequency is approximately 700 Hz. The duty cycle of the Tone output pulses is approximately 3%. This signal suitably buffered may be used to drive a speaker, eliminating the need for mechanical buzzers or external alarm oscillators. Unless the alarm is disabled, the Tone output lasts for one hour after coincidence is detected.

The alarm is enabled while the (AE) switch in the input matrix is closed. To disable the alarm the (AE) switch should be opened. After the alarm is disabled, it may be immediately enabled again in order to utilize the 24 hour capability.

The Snooze feature provides a temporary reset to allow "sleep over". When the (SN) switch is momentarily closed, the Tone output ceases for a period of seven minutes. After this period the Tone output becomes active again unless the alarm has been disabled. This temporary reset may be utilized repeatedly up to one hour.

Either a 12 or 24 hour display may be selected by the (24) switch located at the intersection of the D3 and KA lines in the input matrix. When the (24) switch is closed a 24 hour display sequence from 00:00:00 to 23:59:59 is selected. When the (24) switch is open or absent a 12 hour display mode is selected.

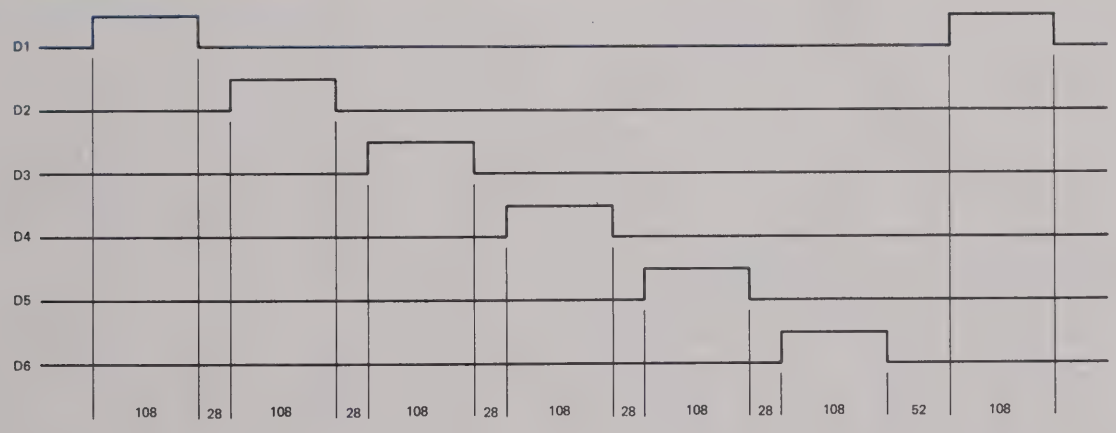
An AM output is provided to distinguish between AM and PM during 12 hour display. The AM output is at a logical one to indicate AM and is at a logical zero to indicate PM. This output switches logic levels every 12 hours in both 12 and 24 hour display modes.

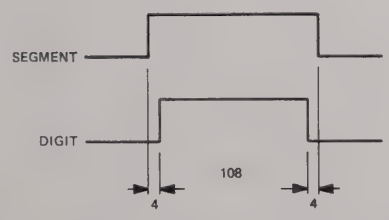
The (50) switch located at the intersection of the D3 and KB lines in the input matrix should be closed for operation from a 50 Hz reference frequency. The (50) switch should be omitted or left open for operation from a 60 Hz reference frequency.

A 1 Hz output is also provided as a time reference signal or it may be used to blink an indicator as an indication that the clock is counting, if the seconds and tens of seconds digits are not displayed. This 1 Hz output is modulated by digit strobe D4 to maintain constant relative intensity between the blinking indicator and the remainder of the display.

Six sequential digit strobes identify the segment information being presented. Figure 2 shows the digit strobe timing and the timing relationship between the digit and segment data.

DIGIT AND SEGMENT TIMING





NOTES:

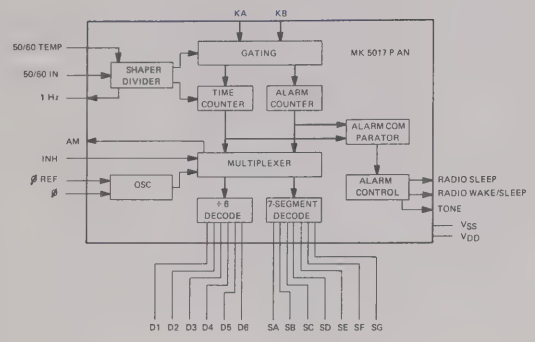
1. TIMES SHOWN ARE IN CLOCK PERIODS.

FIGURE 2

MOSTEK **MK 5017 AN**

Digital Clock Radio Clock

FUNCTIONAL DIAGRAM



INPUT MATRIX

	D6	D5	D4	D3	D2	D1
KA	TS	H	SN	24	SL4	SL
KB	AS	M	AE	50	SL2	SL1

TS – TIME SET
AS – ALARM SET
H
M – USED TO SET HOURS, MINUTES, TENS OF MINUTES
SN – SNOOZE
AE – ALARM ENABLE
24 – 24 HOUR DISPLAY SELECT
50 – 50 Hz INPUT SELECT
SL1, SL2, SL4 } SLEEP CODE
SL – SLEEP

MOS/LSI DIGITAL CLOCK WITH RADIO CONTROL

MK 5017 AN

VSS	1	28	50/60 TEMP
VDD	2	27	50/60 IN
D1	3	26	KA
D2	4	25	KB
D3	5	24	RADIO SLEEP
D4	6	23	RADIO WAKE/SLEEP
D5	7	22	TONE
D6	8	21	N.C.
SG	9	20	1 Hz
SF	10	19	Ø REF
SE	11	18	Ø
SD	12	17	INH
SC	13	16	AM
SB	14	15	SA

FEATURES

- Radio wake
- Radio sleep delay
- Snooze control
- Display inhibit
- Alarm with 24 hour operation
- Alarm tone generated on-chip
- AM/PM indication
- 1 Hz output

DESCRIPTION

Time may be set in the Run mode while the clock circuit is counting or the clock may be set in the Time Set mode while the counters are stopped. Contents of the time counters is displayed in both the Time Set and Run modes. The clock is in the Time Set mode when the (TS) switch located at the intersection of the KA and D6 lines in the input matrix is closed. In the Time Set mode the time counters are stopped and the seconds and tens of seconds digits are reset to zero.

The clock is in the Run mode when both the (TS) and the Alarm Set (AS) switches are open. In the Run mode, counters less significant than the one being set continue counting.

Switches (M) and (H) in the input matrix are closed to cause individual digits to be incremented. The (M) switch causes the minutes digit to be incremented. The (H) switch causes the hours digits to be incremented. Closing both the (H) and (M) switches simultaneously causes the tens of minutes digit to be incremented. Incrementing of a selected digit occurs at a 2 Hz rate and with the exception of the tens of hours digit, digits more significant than the one being set will not increment.

In order to accurately set the time to the nearest second the clock should be placed in the Time Set mode. After setting the time ahead, the clock should then be returned to the Run mode at the proper time in order to start the clock.

The clock must be placed in the Alarm Set mode by closing the (AS) switch to set the alarm. In the Alarm Set mode the time counters continue timekeeping and the contents of the alarm counter is displayed. The alarm may be set to the nearest minute by manipulating the (H) and (M) switches in the same manner as when setting the time.

Both the time counters and the alarm counters have an AM/PM indication which allows the time and the alarm to be set on a 24 hour basis, rather than a 12 hour basis.

The Tone output occurs when coincidence between the alarm counters and the time counters is detected internally, if the alarm is enabled. The Tone output signal is a pulse train whose nominal frequency is equal to the frequency of the scan oscillator divided by 140 and modulated at a 1 Hz rate. For a scan rate oscillator frequency of 100 KHz the Tone output frequency is approximately 700 Hz. The duty cycle of the Tone output pulses is approximately 3%. This signal suitably buffered may be used to drive a speaker, eliminating the need for mechanical buzzers or external alarm oscillators. Unless the alarm is disabled, the Tone output lasts for one hour after coincidence is detected.

The alarm is enabled while the (AE) switch in the input matrix is closed. To disable the alarm the (AE) switch should be opened. After the alarm is disabled, it may be immediately enabled again in order to utilize the 24 hour capability.

The Snooze feature provides a temporary reset to allow "sleep over". When the (SN) switch is momentarily closed, the Tone output ceases for a period of seven minutes. After this period the Tone output becomes active again unless the alarm has been disabled. This temporary reset may be utilized repeatedly up to one hour.

Either a 12 or 24 hour display may be selected by the (24) switch located at the intersection of the D3 and KA lines in the input matrix. When the (24) switch is closed a 24 hour display sequence from 00:00:00 to 23:59:59 is selected. When the (24) switch is open or absent a 12 hour display mode is selected.

An AM output is provided to distinguish between AM and PM during 12 hour display. The AM output is at a logical one to indicate AM and is at a logical zero to indicate PM. This output switches logic levels every 12 hours in both 12 and 24 hour display modes.

The (50) switch located at the intersection of the D3 and KB lines in the input matrix should be closed for operation from a 50 Hz reference frequency. The (50) switch should be omitted or left open for operation from a 60 Hz reference frequency.

A 1 Hz output is also provided as a time reference signal or it may be used to blink an indicator as an indication that the clock is counting, if the seconds and tens of seconds digits are not displayed. This 1 Hz output is modulated by digit strobe D4 to maintain constant relative intensity between the blinking indicator and the remainder of the display.

Radio sleep time is selected by application of a binary code to the three sleep time select switches, SL1, SL2, and SL4. The sleep times that may be selected and the codes for selecting them are shown below.

RADIO SLEEP TIME TABLE

SLEEP TIME	SELECTION CODE		
	SL4	SL2	SL1
10 MIN	0	0	0
20 MIN	0	0	1
30 MIN	0	1	0
40 MIN	0	1	1
50 MIN	1	0	0
60 MIN	1	0	1
90 MIN	1	1	0
120 MIN	1	1	1

0 —AN OPEN SWITCH

1—A CLOSED SWITCH

After selecting the desired time, the Sleep switch (SL) is closed. This starts the proper interval and causes the RADIO SLEEP and RADIO WAKE/SLEEP outputs to switch to a logical zero. To terminate the count before the end of the sleep time, the SL switch is opened. If the SL switch is closed again, the selected sleep interval begins again.

The RADIO WAKE/SLEEP (RWS) output also switches toward V_{DD} whenever coincidence between the time and alarm counters is detected, if the Alarm Enable switch (AE) is closed. RWS remains at a logical zero for one hour after detection of coincidence and then switches to a logical one, toward V_{SS}.

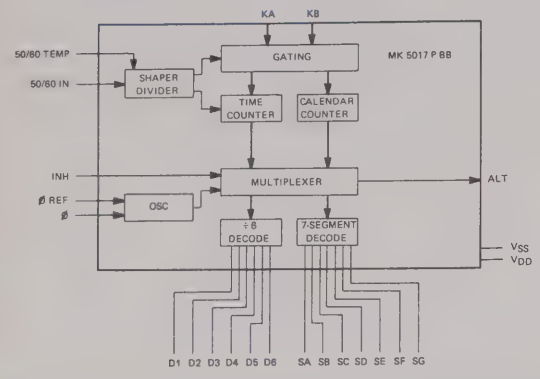
An inhibit input is provided to disable the digit and segment outputs so that they do not switch to V_{SS}. This input may be used to "wire or" multiple chips together. The output transistors are disabled when the INH input is connected to V_{SS}.

Six sequential digit strobes identify the segment information being presented. Figure 2 shows the digit strobe timing and the timing relationship between the digit and segment data.

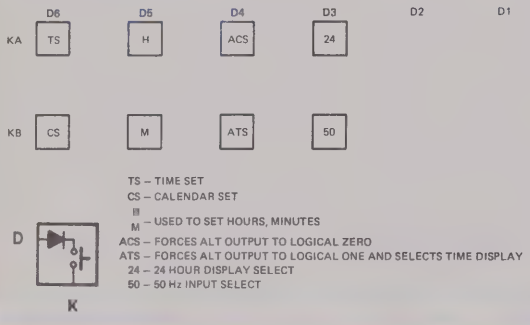
MOSTEK **MK 5017 BB**

Digital Clock/Calendar

FUNCTIONAL DIAGRAM

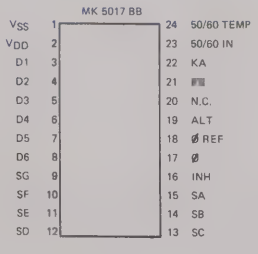


INPUT MATRIX



TS – TIME SET
CS – CALENDAR SET
H
M – USED TO SET HOURS, MINUTES
ACS – FORCES ALT OUTPUT TO LOGICAL ZERO
ATS – FORCES ALT OUTPUT TO LOGICAL ONE AND SELECTS TIME DISPLAY
24 – 24 HOUR DISPLAY SELECT
50 – 50 Hz INPUT SELECT

MOS/LSI DIGITAL CLOCK/CALENDAR



FEATURES

- **Alternating time/calendar display**
- **Display inhibit**

DESCRIPTION

Time may be set only in the Time Set mode. Contents of the time counter are displayed in the Time Set mode and the clock continues counting. The clock is in the Time Set mode when the (TS) switch, located at the intersection of the KA and D6 lines in the input matrix, is closed.

Switches (M) and (H) in the input matrix are closed to cause individual digits to be incremented. The (M) switch causes the minutes digit to be incremented. Closing the (H) switch causes the hours digit to be incremented. Closing the (H) and (M) switches simultaneously causes the tens of minutes digit to be incremented in the Time Set mode. Incrementing of a selected digit occurs at a 2 Hz rate. With the exception of the tens of hours digit, digits more significant than the one being set will not increment.

The clock must be placed in the Calendar Set mode by closing the (CS) switch in the input matrix to set the calendar. In the Calendar Set mode the contents of the calendar counter are displayed. When the (M) switch in the input matrix is closed in the Calendar Set mode, the days digit is incremented. Closing the (H) switch causes the months digit to be incremented. Closing both the (H) and (M) switches simultaneously has no effect in the Calendar Set mode. Incrementing of the digits being set occurs at a 2 Hz rate. Digits more significant than the one being set will increment.

When the day is changed during calendar setting, the time display resets to the AM portion of the day. Thus, the date continues to change at 12:00 A.M. instead of noon.

The clock is in the Run mode when both the (TS) and the alarm set (AS) switches are open. Neither the time counter nor the calendar counter can be set in the Run mode.

An inhibit input is provided to disable the digit and segment outputs so that they do not switch to V_{SS}. This input may be used to

"wire or" multiple clock circuit outputs together. A logical one on the inhibit input disables the outputs.

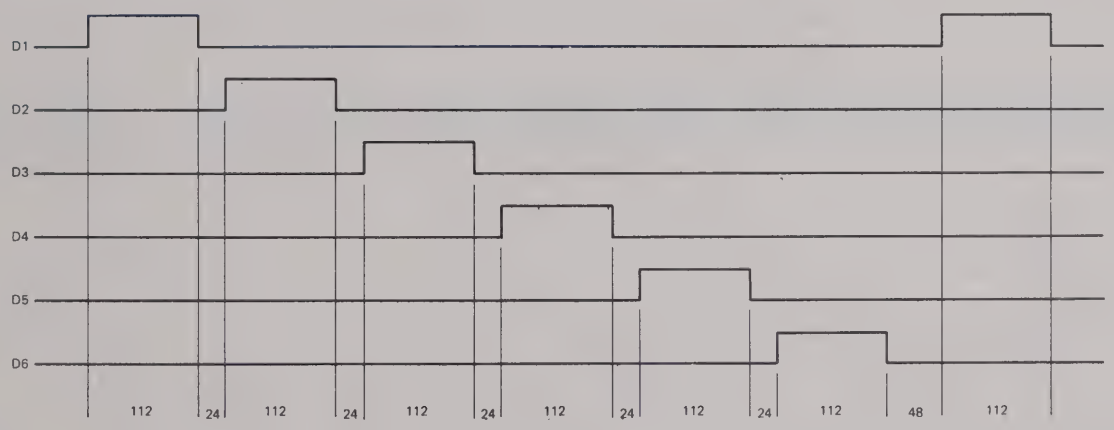
The ALT output indicates whether time or date is being displayed in the Run mode. While time is being displayed the ALT output is at a logical one. In either the Time Set or Calendar Set modes the ALT output continues alternating between a logical one and a logical zero. The ALT output is forced to remain at a logical one when the Alternate Time Set switch (ATS) is closed. Only time is displayed when the (ATS) switch is closed. When the Alternate Calendar Set switch (ACS) is closed, the ALT output is forced to remain at a logical zero.

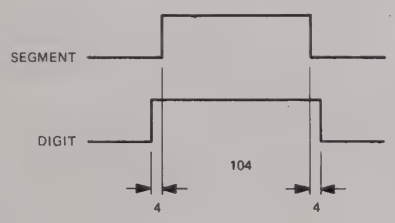
Closing the (24) switch located at the intersection of the D3 and KA lines in the input matrix converts the display to a 24 hour sequence, from 00:00:00 to 23:59:59. Leaving this switch open results in 24 hour operation with the display showing a 12 hour sequence. Closing the (24) switch during the calendar display will cause incorrect months to be displayed. If a 24 hour alternating clock/calendar display is desired, the ALT output may be used to operate a semiconductor (24) switch. Thus a 12 hour format may be selected for calendar display and a 24 hour display selected for time display.

Closing the 50/60 Hz (50) switch located at the intersection of the D3 and KB lines in the input matrix allows a 50 Hz reference frequency to be used. When the (50) switch is open, a 60 Hz reference frequency should be used.

Six sequential digit strobes identify the segment information being presented. Figure 3 shows the digit strobe timing relationship between the digit and segment data.

DIGIT AND SEGMENT TIMING





NOTES:

1. TIMES SHOWN ARE IN CLOCK PERIODS.

FIGURE 3

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE

(All voltages relative to V_{SS})

Supply Voltage Range	
V_{DD}	+0.3 to −20 Volts
Input Voltage Range	
KA, KB	+0.3 to −20 Volts
1NH, 50/60 IN, TEMP, Ø	+0.3 to −20 Volts
Output Voltage Breakdown	
D1–D6, SA–SG, AM	−35 Volts
1 Hz, RS, RSW, TN, Ø Ref, ALT	−25 Volts
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to 150°C

RECOMMENDED OPERATING CONDITIONS

(0°C to +70°C—All voltages relative to V_{SS})

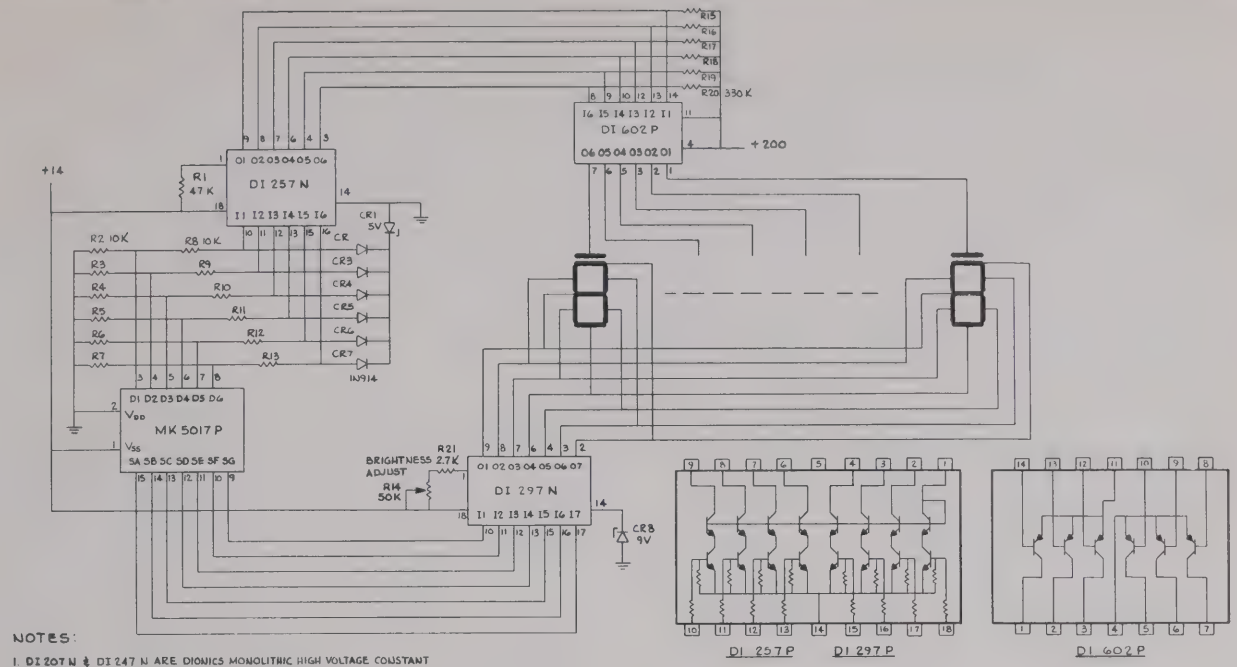
PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Operating Voltages V_{DD}	−11.0		−18.0	Volts	
Input Logic Levels					
KA, KB					
"1" Logic Level	− 4.0		+ 0.3	Volts	
"0" Logic Level	V_{DD} +1.0		−35	Volts	
50/60 In, Temp, Ø					
"1" Logic Level	− 3.0		+ 0.3	Volts	
"0" Logic Level	V_{DD} +0.3		−20	Volts	
INH					
"1" Logic Level	− 1		+0.3	Volts	
"0" Logic Level	− 5		V_{DD}	Volts	
Scan Oscillator Frequency (using external driver)	25		100	KHz	

ELECTRICAL CHARACTERISTICS—5017 AA/AN/BB

($11V \leq V_{DD} \leq 18V$; $0°C \leq T_A \leq 70°C$)

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Output Current					
D1–D6, 1 Hz, ALT					
"1" Logic Level	8			mA	3
"0" Logic Level					2
SA–SG, AM					
"1" Logic Level	200			µA	4
"0" Logic Level					2
TN, RSW, RS					
"1" Logic Level	0.8			mA	5
"0" Logic Level	50			µA	6
Supply Current, I_{DD}		10	16	mA	
Leakage, D1–D6, SA–SG, AM			10	µA	7
Leakage, 1 Hz, ALT			10	µA	8
Scan Oscillator Frequency	60		210	KHz	1
Input Current, KA, KB			0.5	mA	9
Input Current, INH			1.0	mA	10

Note 1 RØ = 18K, CØ = 51PF, $T_A = 25°C$
Note 2 External Resistor Required
Note 3 Output voltage equal to V_{SS}−3.0V
Note 4 Output voltage equal to V_{SS}−0.5V
Note 5 Output voltage equal to V_{SS}−2.0V
Note 6 Output voltage equal to V_{DD}+4.0V
Note 7 $V_{DD} = V_{SS} = 0$ volts, output voltage equal to −35 volts
Note 8 $V_{DD} = V_{SS} = 0$ volts, output voltage equal to −20 volts
Note 9 Input voltage equal to V_{SS}−3.0V
Note 10 Input voltage equal to V_{SS}



NOTES:

1. DI 207 N & DI 247 N ARE DIONICS MONOLITHIC HIGH VOLTAGE CONSTANT CURRENT 7 SEGMENT DISPLAY DRIVERS.
2. DI 602 P IS DIONICS HIGH VOLTAGE SILICON PNP TRANSISTORS ARRAYS

FIGURE 9

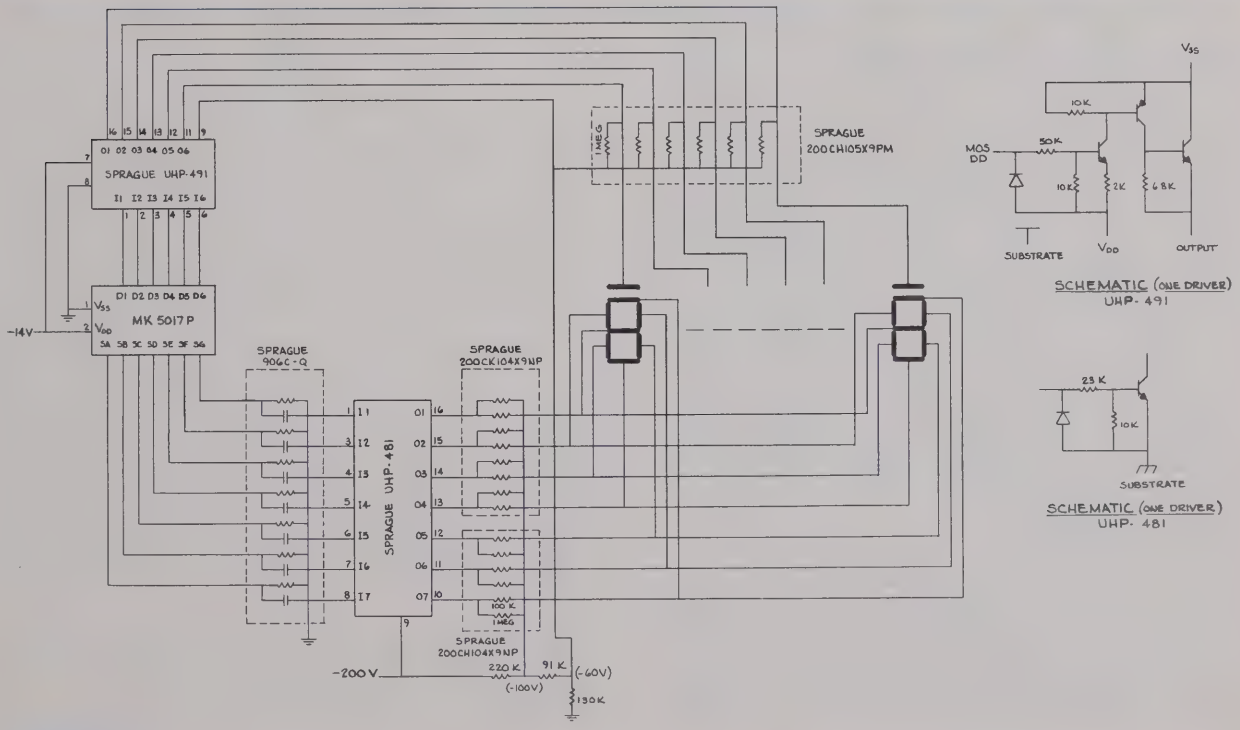


FIGURE 10

LED DISPLAYS

Several circuits may be developed for interfacing the MK 5017 P clock circuits to seven segment Light Emitting Diode (LED) displays. LED displays fall into two major categories, the common anode and the common cathode displays. LED displays may be further subdivided into the low current displays and the high current displays. This division is a function of the display size since the larger digits require more current than the smaller ones.

Figure 11 shows an interface circuit which may be used to interface common cathode LED displays which require less than 10 mA average forward segment current to the MK 5017 P clock circuits. Since the clock digit outputs are multiplexed sequentially with a duty cycle for any one digit of approximately 13%, in order to drive a LED display segment with a forward segment current equivalent to an average forward segment current of 10 mA requires a pulsed current of (10 mA ÷ 0.1285) or 77 mA. In figure 11 a 2N4401 NPN transistor is used as a saturating emitter follower to provide the necessary 77 mA current pulse to drive the display segments. Since the collectors of the 2N4401 segment driver transistors are connected to the +7.5 Vdc display supply voltage the transistors are driven into saturation when the MK 5017 P open drain segment output transistors switch ON pulling the digit outputs near V_{SS} (+14 Vdc). Series 2K current limiting resistors prevent excessive current drain from the clock segment output transistors. The base of each of the segment driver transistors is returned to ground by a 100K pulldown resistor when the MK 5017 P segment output transistors are turned OFF.

Each of the common cathodes of the display require a driver that is capable of sinking (7 x 77 mA) or 540 mA. Motorola MPSU45 NPN darlington transistors may be used as digit drivers since they are rated at 2A maximum collector current. At a collector current of 540 mA the MPSU45 digit drivers have a current gain of approximately 25,000. Series 33K current limiting resistors are connected between the MK 5017 P digit output pins and the base of each MPSU45 to allow the digit outputs of the clock to swing over the required range from (V_{SS} −3.0 volts) to (V_{DD} +1.0 volts). Base pulldown resistors of 56K insure cutoff of the digit drivers when the MK 5017 P digit output transistor is turned OFF.

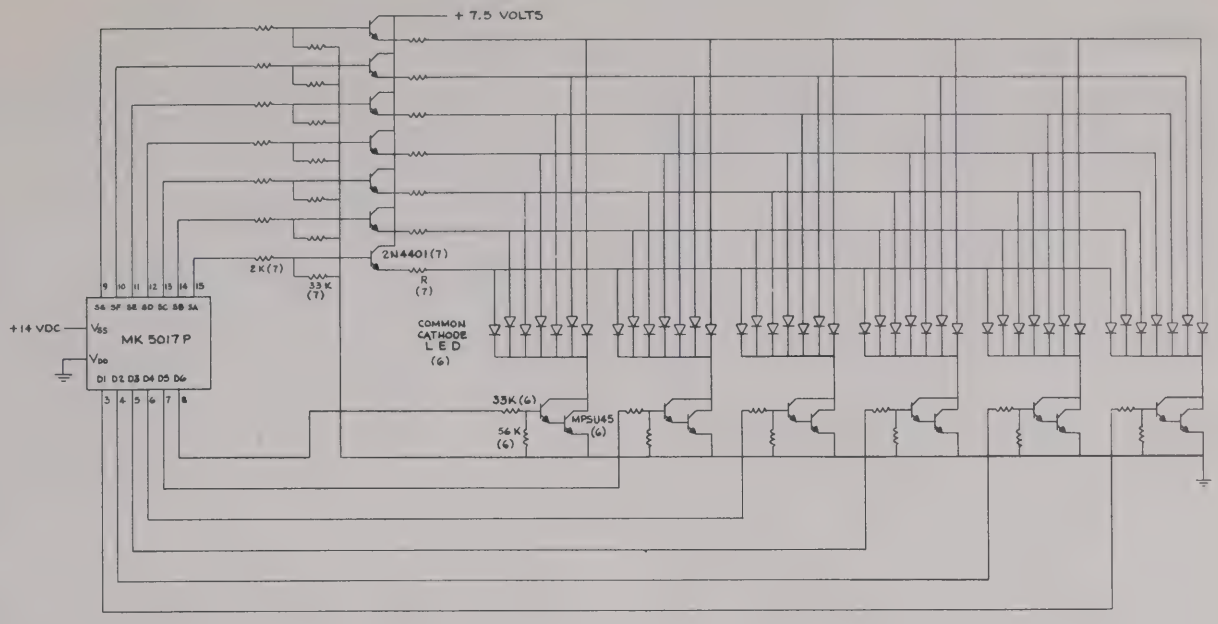
Display segment current is limited to the selected value by current limiting resistors connected in series with each of the display segment bus lines. The value of this resistor may be determined from the expression below.

$$R = \frac{V_{DISPLAY\ SUPPLY} - V_{CE_{SAT\ (2N4401)}} - V_{CE_{SAT\ (MPSU45)}} - V_{F_{LED}}}{I_{SEG_{PEAK}}} \qquad \text{EQ. 1}$$

$$\text{Example: } R = \frac{7.5 - 0.2 - 1.0 - 1.7}{77.8} \approx 59\Omega$$

The darlington transistor digit drivers shown in figure 11 may be replaced by SCRs as shown in figure 12. In this figure Texas Instruments TIC44 SCRs are used as the display digit drivers. When the MK 5017 P digit outputs are pulled high near V_{SS} by the digit output transistors the TIC44 is triggered into conduction. This SCR requires a gate trigger current of 200 μA and a gate trigger voltage of 0.8 volt. A 3K series current limiting resistor limits the MK 5017 P digit output current to allow the required voltage swing from (V_{SS} −3.0 volts) to (V_{DD} +1.0 volts) on the clock digit output pins. A 10K pulldown resistor connected from the gate of each SCR to ground prevents the SCR from being triggered into conduction when the MK 5017 P digit output transistor is turned off.

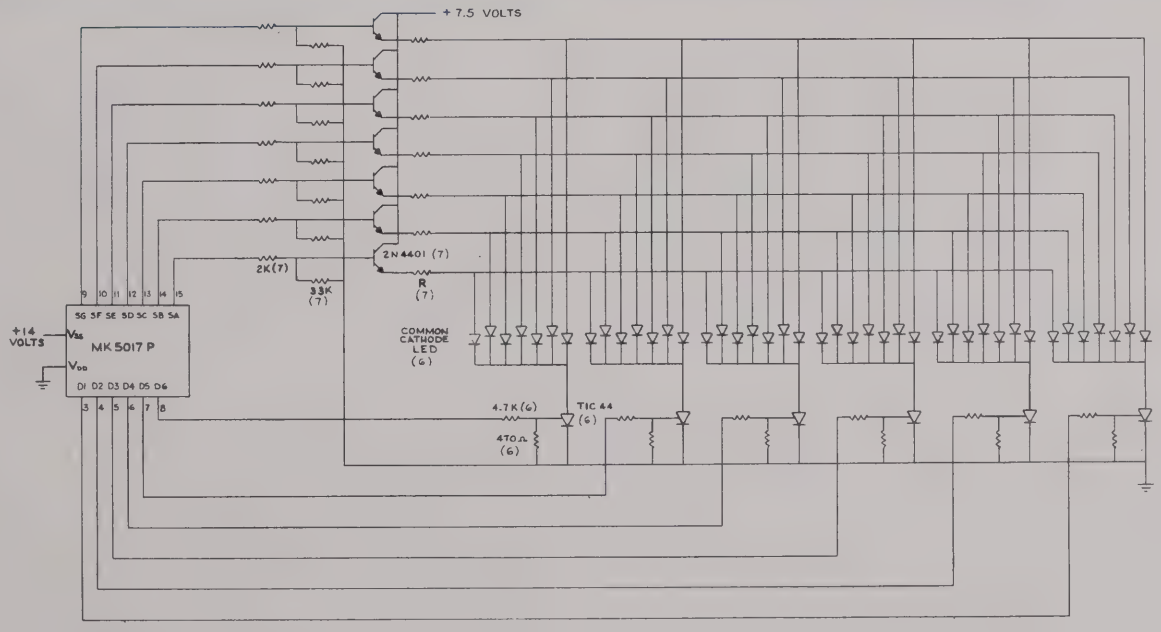
Once triggered by the digit strobe the SCRs remain on throughout the digit ON time. Since there is no holding current during the interdigital blanking period



NOTES:

1. RESISTORS ARE 1/4 W., UNLESS OTHERWISE SPECIFIED.
2. I_F LESS THAN 10 MA.

FIGURE 11



NOTES:

1. I_F LESS THAN 10 MA.
2. RESISTORS ARE 1/4 W., UNLESS OTHERWISE SPECIFIED.

FIGURE 12

LED DISPLAYS

the SCR turns OFF between digit strobes. The value of the segment current limiting resistor may be calculated from an expression similar to that used for the interface circuit in figure 11.

$$R = \frac{V_{DISPLAY\ SUPPLY} - V_{CE_{SAT\ (2N4401)}} - V_{F_{SCR}} - V_{F_{LED}}}{I_{SEG_{PEAK}}} \qquad \text{EQ. 2}$$

$$\text{Example: } R = \frac{7.5 - 0.2 - 1.4 - 1.7}{77.8\ mA} = 54\Omega$$

In order to drive a common cathode LED display requiring an average forward segment current of 10 mA to 20 mA, Motorola MPSU45 NPN darlington transistors may be used to drive the display digits and MPSA13 darlington transistors may be used to drive the display segments, see figure 13. If the average forward segment current for the chosen LED is 20 mA, the pulsed segment current for a multiplexed clock display is approximately 154 mA and the pulsed digit current is about 1 A. MK 5017 P digit output current available for the display is equal to the total output of 8 mA minus the 0.5 mA required by the KA and KB inputs or 7.5 mA, a digit driver transistor with a gain of 145 at a collector current of 1 A is required. The MK 5017 P segment output current is specified as 0.2 mA with a voltage drop not greater than 0.5 volt so a segment driver transistor with a gain of 780 at a collector current of 154 mA is required.

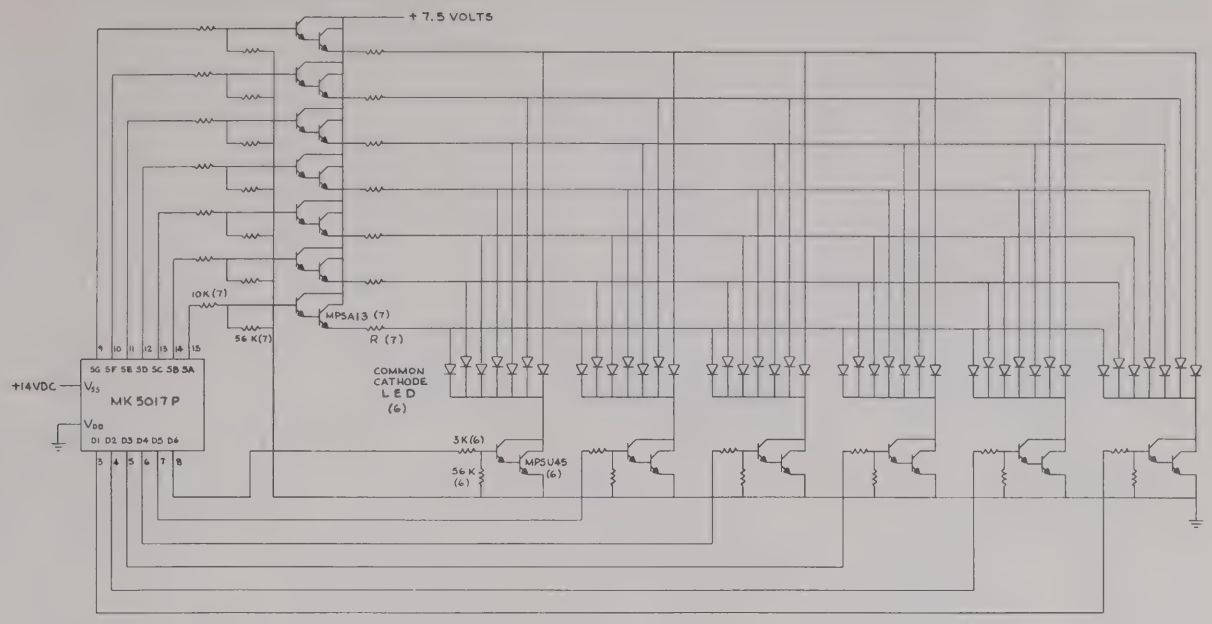
As shown in figure 14 the MPSU45 darlington transistors used as digit drivers may be replaced by Texas Instruments TIC44 SCRs. As each of the digits in the display are scanned sequentially, the appropriate SCR associated with a particular digit is triggered. The SCR remains ON, conducting display current until both the digit and segment drivers are turned OFF during the interdigital blanking period between successive digits, then since there is no longer any holding current for the SCR, the SCR turns OFF.

In addition to the discrete common cathode LED interface circuits, the Texas Instruments SN75491 and SN75492 integrated circuit drivers may be used instead. Figure 15 shows a common cathode LED which requires less than 4.5 mA average forward current being driven by the SN75491 segment drivers and the SN75492 cathode drivers. As shown in figure 15, the common of the driver circuits are all connected together and to a reference point which is 5 volts above ground, the 5 volt Zener diode being used to establish a reference point. Because the digit outputs of the MK 5017 P must switch from (V_{SS} −3.0 volts to (V_{DD} +1.0 volt) in order to establish a logical one a logical zero level on the KA and KB inputs, the 75492 digit driver inputs must be able to withstand this same voltage swing. The maximum positive voltage on the SN75492 input pins relative to the common pin is +10 volts. Input pins can withstand a negative voltage relative to the common pin of (−5) volts. Thus if the common voltage pin is at +5 volts relative to V_{DD}, the input swing up from V_{DD} to V_{SS} on the input pins of the SN75492 digit driver will not exceed the maximum operating range. Since the SN75492 digit driver can sink a maximum current of 250 mA, the display may be operated at an average forward segment current of (250 mA ÷ 7) x (0.13) ≈ 4.5 mA.

The SN75491 anode driver may be driven directly from the MK 5017 P clock circuit in the same manner as the SN75492 cathode driver. Display segment current limiting resistors are connected from the common collectors of the SN75491 anode drivers to the V_{SS} supply voltage. The calculation of resistor values required for a display requiring an average forward segment current of 4.5 mA is described below in equation 3.

$$R = \frac{V_{SS} - V_{F\ (SN75491)} - V_{F\ (SN75492)} - V_{F\ LED} - 5\ V}{I_{SEG_{PEAK}}} \qquad \text{EQ. 3}$$

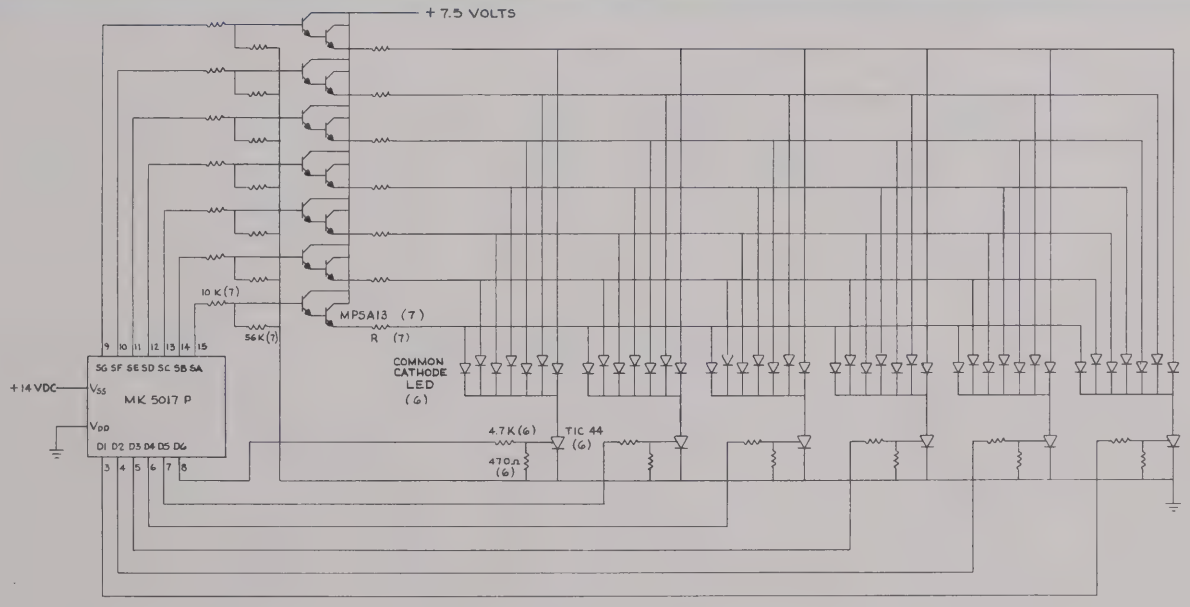
Common anode LED displays requiring an average forward segment current less than 20 mA may be interfaced to the MK 5017 P clock circuit as shown in figure 16. Since the maximum pulsed forward segment current for a display requiring an average forward segment current of 20 mA is 156 mA, the MPSA13 darlington transistors may still be used as segment drivers. Since the digit current is now on the order of approximately 1 A, the MPSU45 darlington transistor or equivalent must be used as a digit driver. The 3.3 K base resistor shown, limits the digit current into the base of the darlington digit drivers. The 56K pull-down resistors connected from the base of the darlington digit driver transistors to ground, insure that the digit drivers are turned OFF when the clock circuit digit output driver transistors are turned OFF. The 10Ω current limiting resistors shown connected in series with each of the segment bus lines are employed to limit the pulsed segment current into the display. The value of these current limiting resistors may be calculated as demonstrated previously.



NOTES:

1. I_F GREATER THAN 10 MA., LESS THAN 20 MA.
2. RESISTORS ARE 1/4 W., UNLESS OTHERWISE SPECIFIED.

FIGURE 13



NOTES :

1. I_F GREATER THAN 10 MA., LESS THAN 20 MA.
2. RESISTORS ARE 1/4 W., UNLESS OTHERWISE SPECIFIED.

FIGURE 14

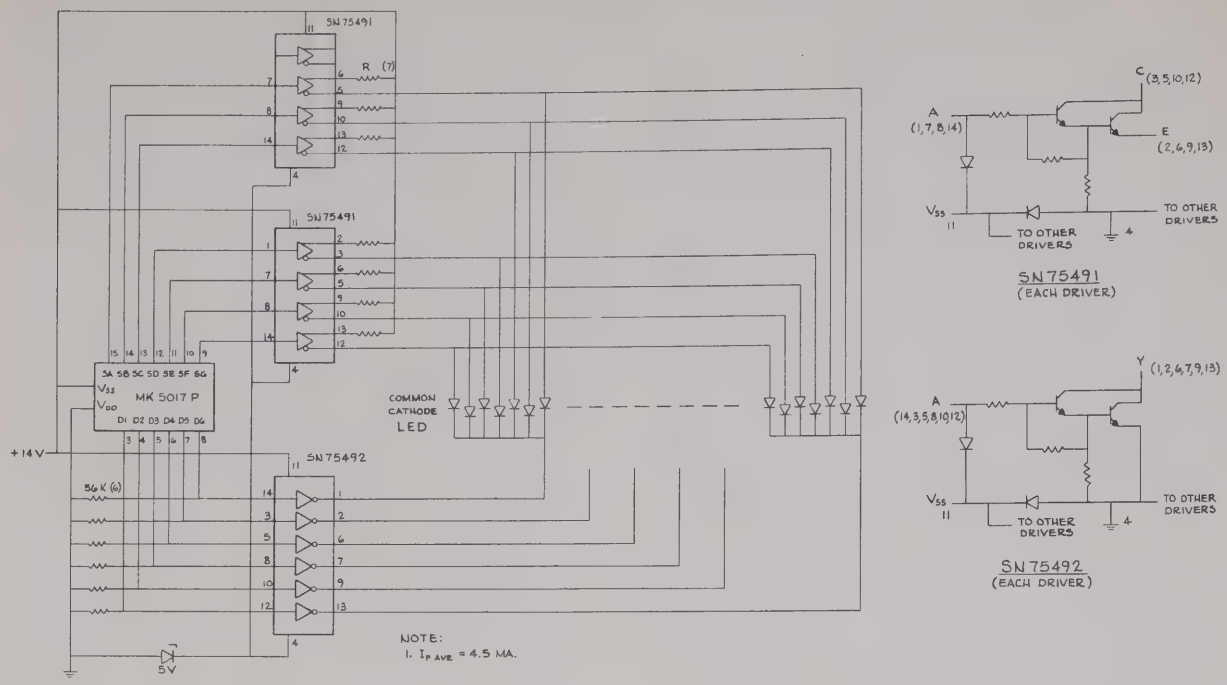


FIGURE 15

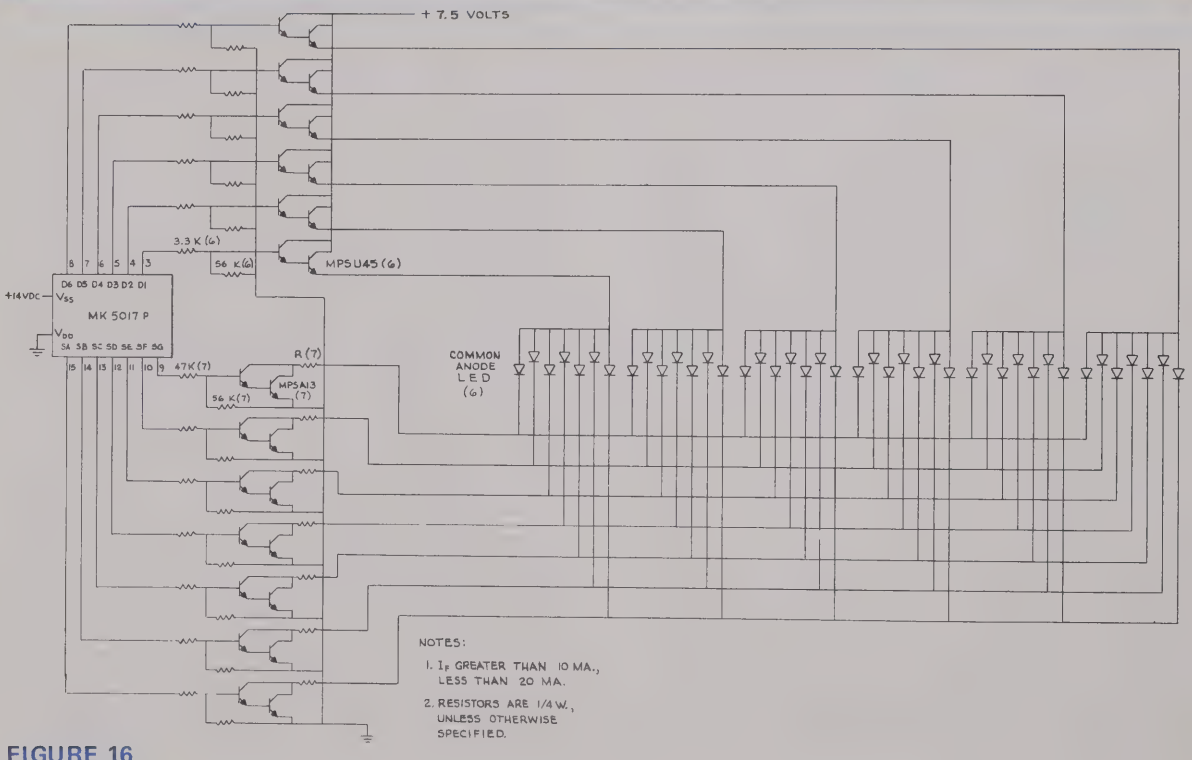
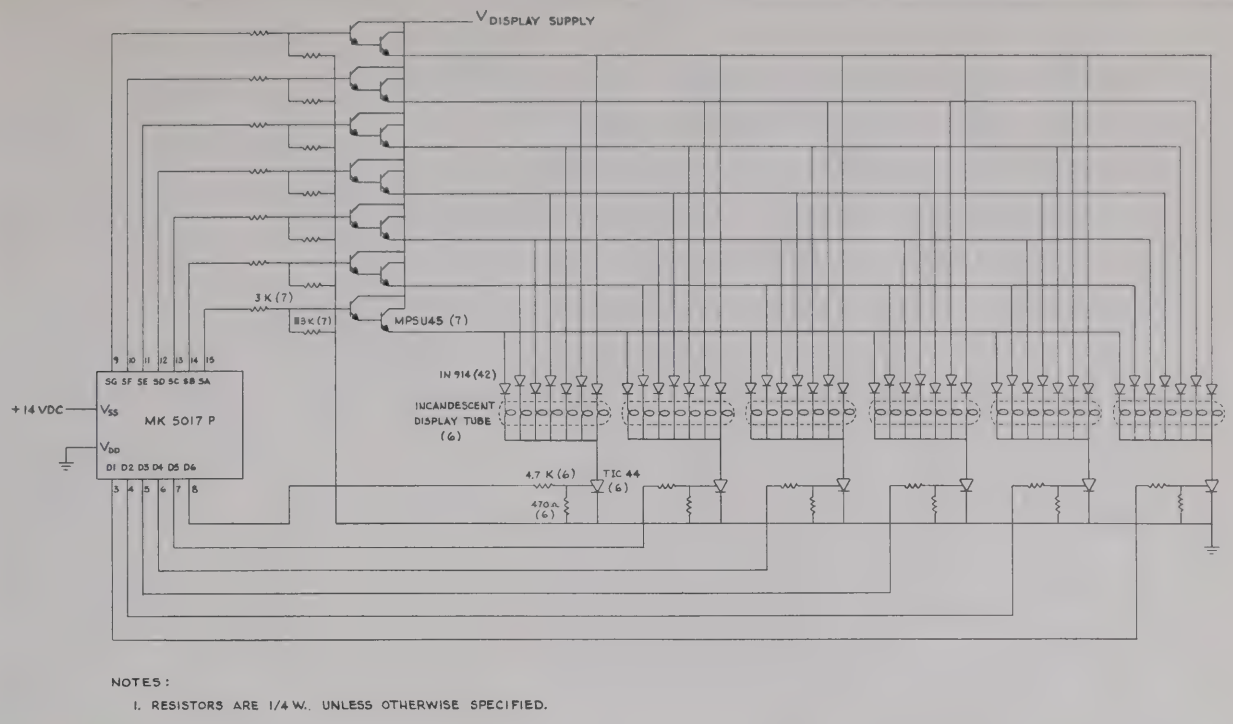


FIGURE 16



NOTES:

1. RESISTORS ARE 1/4 W., UNLESS OTHERWISE SPECIFIED.

FIGURE 17

INCANDESCENT DISPLAYS

Figure 17 shows a circuit suitable for interfacing incandescent display tubes to the MK 5017 P clock circuits. Texas Instruments TIC44 SCRs may be used as digit drivers. The 3K series gate resistors limit the gate current in the SCR. Gate pulldown resistors connected from the gate of each SCR to ground will assure turn off. Each of the seven segment lines is driven by MPSU45 darlington emitter follower transistor. Since the incandescent display tube filaments are bi-directional devices, isolation diodes must be used to prevent "sneak paths" from partially turning on unwanted display segments. For example, assume that the isolation diodes were omitted, from the circuit shown in figure 17. If the segment A driver transistor were turned on during the digit number one strobe, D1, it can be seen that segment A of each of the five remaining display digits would be connected through the remaining segments D through G back to segments B through G of digit no. 1. Since digit no. 1 is enabled and the common side of the digit no. 1 display segment is connected to ground by the digit no. 1 SCR, all the segments A through G on all of the digits would be partially turned on.

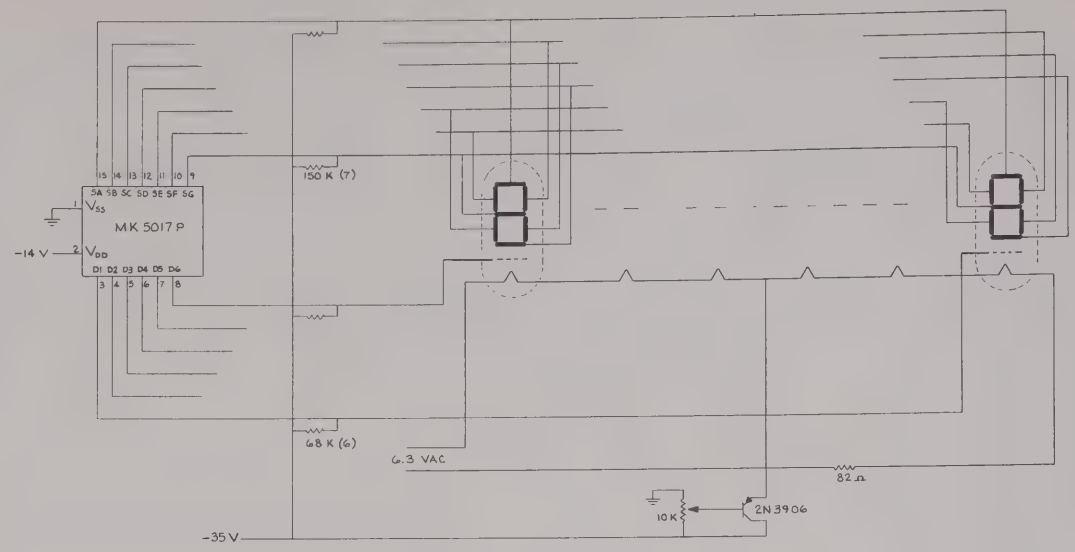


FIGURE 18

FLUORESCENT ANODE TUBE DISPLAYS

As shown is figure 18 fluorescent anode tubes such as the ISE DG10A and the National Electronics NL-8051 may be driven directly from the MK 5017 P clock circuits. The segments or anodes are connected directly to the MK 5017 P segment outputs. The control grid for each tube is connected directly to the MK 5017 P output pins. The display tube filaments are all connected in a series string and through an 82Ω current limiting resistor to the 6.3 volt winding on a filament transformer. This filament string is biased at about −25 volts (relative to V_{SS}) by transistor Q1 which may be used to provide brightness control for the display.

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MOS Applications Notes

MOSTEK CORPORATION

Applications of Ion-Implanted Depletion-Mode MOS Devices

AN-101/AUG. 1971

SUMMARY

Ion implantation can be used in conjunction with conventional, MOS P-channel processing to create both depletion-mode and enhancement-mode devices on the same monolithic IC. Used in place of conventional MOS load resistors, depletion-mode devices offer constant current operation with resulting performance improvements of speed, power, and operating power supply voltage range. Circuits implemented with depletion-mode loads can be designed to operate from a single +5V power supply. Additionally, linear MOS circuits can be integrated along with digital circuitry on the same chip.

Design concepts have been verified by use of ion-implanted depletion-mode devices in commercially available, production circuits. Costs associated with ion-implanted MOS/LSI compare favorably with other process techniques.

DEPLETION DEVICE FUNDAMENTALS

A depletion-mode field-effect transistor is defined as one which exhibits substantial device current (I_{DSS}) with zero gate-to-source bias (V_{GS}=0V).

An enhancement-mode field-effect transistor is defined as one in which no device current flows (leakage only) when V_{GS} is zero volts. Conduction does not begin until V_{GS} reaches a voltage called the threshold voltage, V_T.

Junction FETs are all depletion-mode devices, whether N or P-channel. MOSFETs, on the other hand, tend to be enhancement-mode when P-channel processing is used, and depletion-mode with N-channel processing. Ion implantation can be used to controllably alter these natural tendencies. Fig. 1 shows how both low-threshold, enhancement devices and depletion devices are created on the same chip. The starting process is standard, <111> high-threshold P-channel. The first implantation step lowers the threshold of all MOS devices on the chip by two volts. A second implantation lowers the threshold of selected devices still further, through zero volts to +5V. This voltage is termed the pinchoff voltage, V_P, to be consistent with depletion device terminology. Selection of depletion devices is achieved by the addition of one extra masking step to the basic process.

The value of I_{DSS} is determined by the geometry of the devices; values of 3 μA to 3 mA are typically used in present designs.

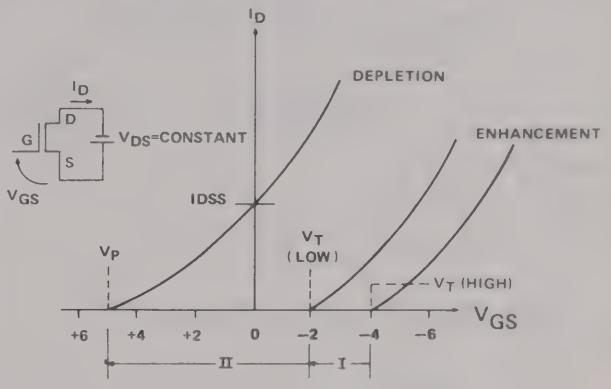

Fig. 1. Threshold voltage reduction by ion implantation

THE DEPLETION DEVICE AS A LOAD ELEMENT

Because a depletion device exhibits current flow for V_{GS}=0V, it can be used as a constant-current load element. Fig. 2 shows several MOS inverter configurations. In both (a) and (b), the gate-to-source voltage of the enhancement load devices varies with output voltage, which should be contrasted with the depletion load in (c).

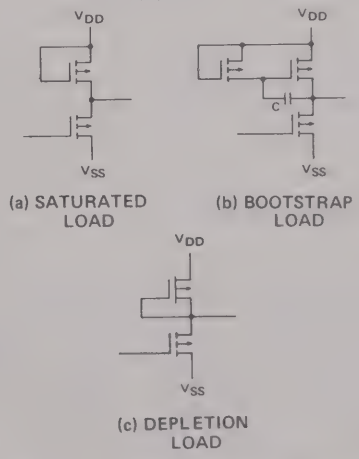

Fig. 2. MOS inverter circuits

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Full supply voltage output swing is achieved only by circuits (b) and (c). The bootstrap circuit of (b) is not stable indefinitely and the output will decay as C discharges, while the depletion-load inverter has a static output. Table 1 compares the speed, area, and gate oxide area (related to yield) of the three inverters. All numbers are normalized with respect to the depletion-load inverter, and represent actual design examples based on: equivalent power dissipation, consistent layout rules, and operation from a 17V supply differential.

TABLE 1 INVERTER COMPARISON

	Propagation Delay	Area	Thin Oxide Area
Depletion Load (c)	1	1	1
Bootstrap Load (b)	3	2.6	12
Saturated Load (a)	6	1.4	2.5

In summary, the depletion-load inverter exhibits the following features:

1. Full supply-voltage swing with static operation
2. Higher speed
3. Smaller size
4. Less gate oxide area

Inverter gain is also greater for a given geometry, due to the higher impedance of the constant-current load.

PERFORMANCE ADVANTAGES OF MOS/LSI USING DEPLETION LOADS

When LSI circuits are fabricated using depletion-mode load devices, a number of performance features can be obtained, some of which are unobtainable with other technologies. Among these are:

Single-supply, +5V Operation

The full power supply swing of depletion-load inverters allows complex MOS circuits to be designed to operate from a single, +5V supply. Such a circuit, shown in Fig. 3, has been fabricated and is now commercially available (as MOSTEK's MK 5002 P). Complexity of this 4-digit, counter/display chip is over 300 logic gates.

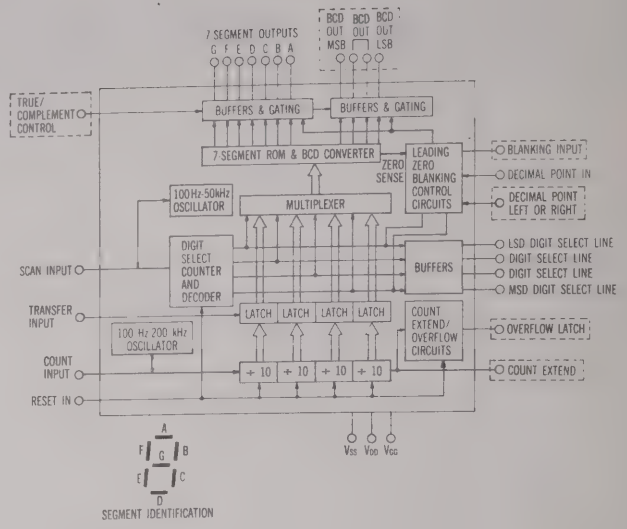


Fig. 3. Low-power MOS/LSI circuit using depletion loads

Power Dissipation

Speed and power can be flexibly traded off during design with depletion loads. The circuit in Fig. 3 dissipates less than 20 mW when operated from a +5V power supply and uses depletion loads with I_{DSS} values as low as 3 μA. Input clock rates up to 250 KHz are acceptable.

Power Supply Tolerance

Circuits fabricated with depletion loads are effectively isolated from supply voltage variations due to the constant-current properties of these loads. For example, the circuit in Fig. 3 will operate from supply voltages from 5 to 20 volts.

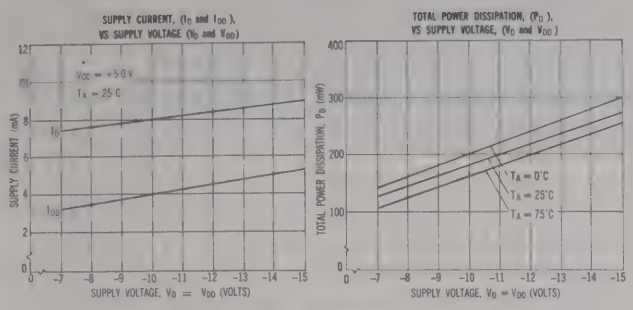
In addition to supply voltage latitude, power supply dissipation varies linearly with supply voltage. If the inverter of Fig. 2 (a) and (b) are subjected to increasing supply voltage, the load current rises so that:

Enhancement load $I_L \sim V_{DD}^{1-2} \therefore P_{diss} \sim V_{DD}^{2-3}$

whereas, if the load is a constant current-source, (Fig. 2c)

Depletion-load $I_L = \text{constant} \therefore P_{diss} \sim V_{DD}$

Fig. 4 shows the actual supply current and power variation of a depletion-load circuit, MOSTEK's MK 4007 P 256 X 1 read/write memory.


SUPPLY CURRENT, (I_D and I_{DD}), VS SUPPLY VOLTAGE (V_D and V_{DD})
V_{CC} = +5.0 V
T_A = 25°C
I_D
I_{DD}
SUPPLY CURRENT (mA)
SUPPLY VOLTAGE, V_D = V_{DD} (VOLTS)
TOTAL POWER DISSIPATION, (P_D), VS SUPPLY VOLTAGE, (V_D and V_{DD})
TOTAL POWER DISSIPATION, P_D (mW)
T_A = 0°C
T_A = 25°C
T_A = 75°C
SUPPLY VOLTAGE, V_D = V_{DD} (VOLTS)

(a) (b)

Fig. 4. Supply current and power dissipation vs. supply voltage for depletion load circuit (MK 4007 P)

Supply Line Noise Susceptibility

Tolerance of a large supply voltage range is equivalent to a high circuit immunity from supply transients.

TTL Compatibility

Depletion devices as constant current load elements are particularly well suited for interfacing the output of MOS/LSI with TTL where a sink to negative supply is employed. In this application, enhancement-only circuits suffer from a loose control of sinking currents. Typical variations are in the order of 6 to 1 for a ± 5% supply tolerance. Use of depletion devices lowers this variation; 2 to 1 for supply variations in excess of ± 30%.

Depletion-load inverters can also be used in an MOS input to provide direct TTL compatibility (0.8V logic 0 level, 2.4V logic 1 level). In this application the high gain of these inverters allows reasonable speed performance with the small TTL output voltage swing, as well as good threshold voltage control.

OTHER APPLICATIONS OF DEPLETION DEVICES IN MOS/LSI

Linear MOS can be fabricated along with digital MOS on the same chip using depletion devices. Fig. 5 shows a differential pair currently used in the sense amplifier of a production circuit (MK 4007 P).

This circuit, cascaded with similar stages, allows small voltages (under 100 mV) to be sensed without speed penalties. Such circuitry can be expected to assume increasingly important roles in products such as large (4K and above) read/write memories which rely on a single transistor, dynamic memory cell.

Simple sinusoidal oscillators and amplifiers can also be fabricated using the circuit in Fig. 5. Zero-crossing detectors, keeping one input at an external ground reference, are still another useful application.

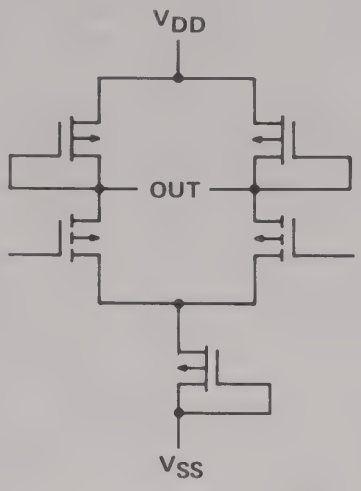


Fig. 5. MOS differential pair using depletion devices

MANUFACTURING COST -- A COMPARISON

When comparing the cost of ion-implanted, depletion-load circuitry to other processes, three factors must be considered:

1. Basic process cost
2. Circuit densities (chip size)
3. Yields

The basic process cost of ion implantation is essentially that of high-threshold, P-MOS plus implant costs, as well as one extra masking step if depletion devices are also created. Current production rates of 100, 2 inch slices/hour have been achieved for implantation, making the added cost of this step relatively unimportant.

Circuit densities, related to chips/slice, are enhanced over the basic P-MOS process when depletion loads are employed. Three reasons contribute to this density improvement:

1. An equivalent performance depletion inverter takes up less than 70% of its enhancement couterpart.

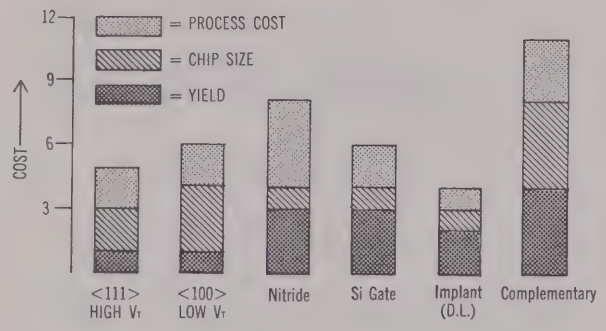
2. The metal area associated with routing an extra supply voltage (V_{GG}), frequently employed in enhancement-only circuitry, is eliminated.

3. More powerful logic gates are available because 4 or 5 devices can be placed in series.

Yields of depletion-mode circuitry are improved over their standard P-MOS counterpart, because the positive effects of threshold voltage controllability and reduced thin oxide area offset the increased process complexity.

Table 2 estimates cost factors of current processes, based on implementing random logic, using a scale of 1 to 4 for the individual cost contributions. The total rating is the sum of these factors, on a scale of 3 to 12, with 3 being the lowest cost.

TABLE 2 PROCESS COST COMPARISON



CONCLUSION

The flexibility of MOS/LSI design using ion-implanted, depletion-mode devices will have a strong impact in a variety of market areas. Complementary MOS will be seriously challenged in the low-power market area, particularly where high density and low cost are important. Where wide supply voltage variation is a problem, such as automotive and battery-operated equipment applications, depletion circuitry offers an attractive MOS approach. Memory products, as well as traditionally non-MOS applications, will strongly benefit by the linear capability available using depletion devices.

ACKNOWLEDGMENT

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by
GORDON HOFFMAN, *Applications Manager*
MOSTEK Corporation

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Using the MK 5009 P MOS Counter Time-Base Circuit

AN-104 / Oct. 1972

DIGITAL FREQUENCY METER

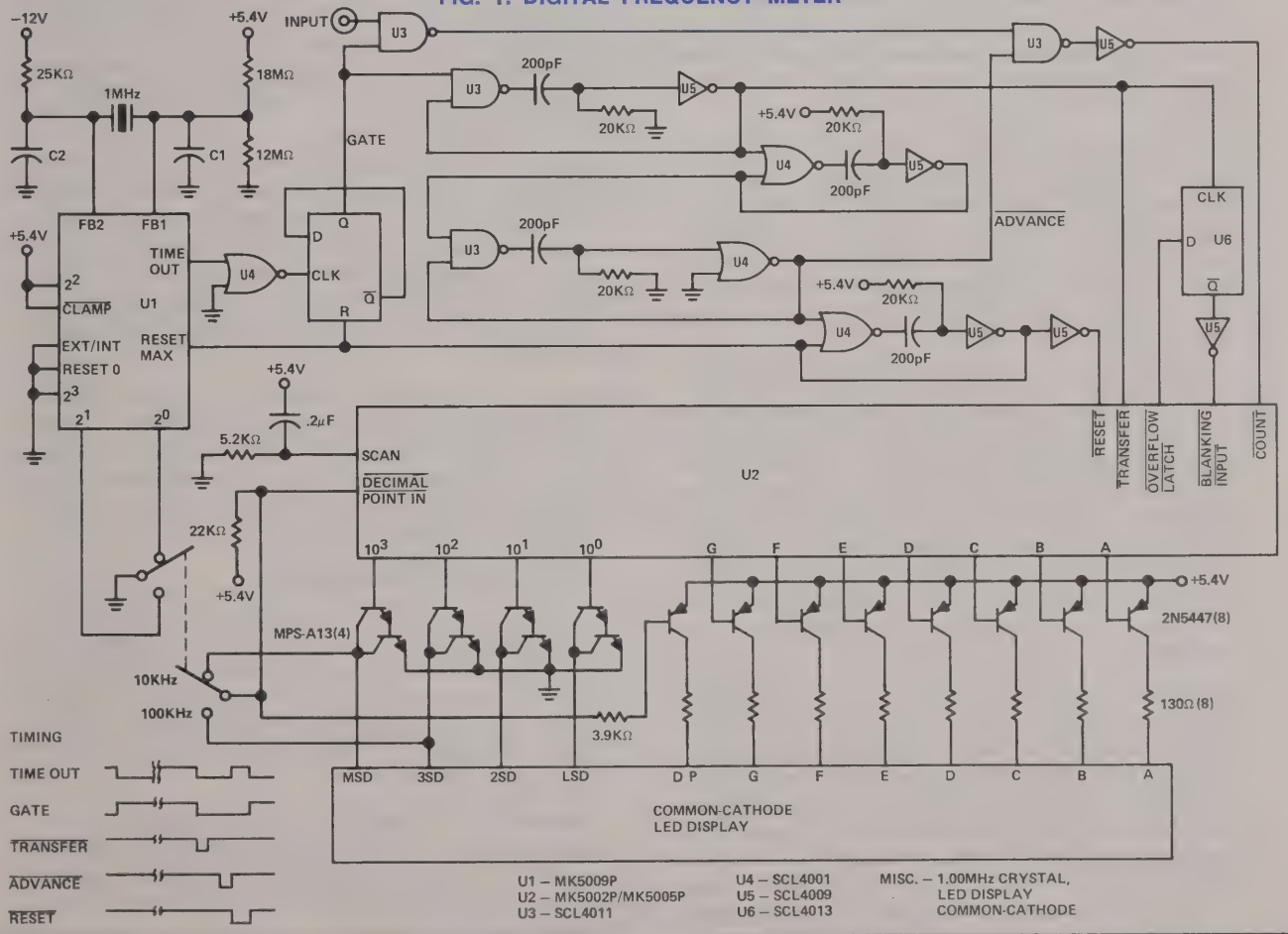
A 100 KHz frequency meter which can be battery operated is illustrated schematically in Fig. 1. The +5.4V power required is supplied by four C cells and a series diode. Since most of the 200 mA required is used in the LED display, it is advantageous to employ a "push-to-read" function on the meter. This is easily accomplished by using either a MOSTEK MK 5002 P or MK 5005 P as the counting device and display driver. If an unconditional reset is applied to the U-6 flip-flop to be released only when the display is to be read, the display normally will be blanked.

The circuit's input responds to a +5V signal. A more general purpose front end, if desired, could be added to the NAND gate U3. The range of the meter could also be expanded by using decade prescalers at the input.

The timing diagram in Figure 1 also shows the interface timing between the MK 5009 P and MK 5002 P. Basic C/MOS one-shots are used to conserve power; but if battery operation is not required, standard TTL one-shots can be used. The four one-shots generate the following times; transfer pulse width (at the end of a measurement period); time delay between the transfer pulse and count negative edge; count negative edge; and reset pulse width. To obtain an accurate time-out interval on the MK 5009 P, a flip-flop is used to count two consecutive negative edges of the Time-Out output.

This simple circuitry gives a 4-digit frequency meter with crystal-controlled accuracy, typically requiring 8 mA from the positive supply and 5 mA from the negative supply, excluding display power.

FIG. 1: DIGITAL FREQUENCY METER



U1 – MK5009P
U2 – MK5002P/MK5005P
U3 – SCL4011
U4 – SCL4001
U5 – SCL4009
U6 – SCL4013
MISC. – 1.00MHz CRYSTAL, LED DISPLAY COMMON-CATHODE

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PULSE GENERATOR

An extremely versatile pulse generator requiring few components is easily built using the MK 5009 P. Three MK 5009 P circuits are used, as shown in Fig. 2, to provide the three essential pulse generator elements: (1) a frequency source to determine pulse repetition rate; (2) a variable time delay; and (3) a pulse width generator.

This circuit provides repetition rates from 0.1 Hz to 100 kHz with delay times and pulse widths from 10μs to 10 seconds. Range selection is obtained by selecting the appropriate divider, so that only three RC circuits are required. This eliminates the requirement for a different RC combination for each decade, commonly found in commercial instruments. Decade selection is accomplished by a binary code at the inputs to each MK 5009 P, which could be provided by a coded rotary or thumbwheel switch. The vernier control is a 500K potentiometer. A 100K potentiometer is used as a trimmer for initial calibration.

External TTL control logic is used to capture the accurately controlled negative edges as they emerge from each MK 5009 P. The Reset and Clamp Inputs allow synchronization and first-cycle accuracy from the time-base circuits.

Other features can be added to the basic circuitry shown in Fig. 2. For example, the output amplitude can be made adjustable by using high-voltage, open-collector TTL circuitry with potentiometer control for amplitude. An extra position can be used on the frequency selection switch for an external trigger source. This trigger source should be connected to the first control D-type latch in lieu of the output from the 5009 (1). The frequency range may even be extended to 1.0 MHz with time delays reduced to 1μs, although some loss in RC stability would occur since the recommended data sheet frequency had been exceeded.

DIGITALLY-PROGRAMMABLE ONE-SHOT

Using the MK-5009 in the circuit shown in Fig. 3 results in a very accurate one-shot which is digitally programmable. Four decades of thumbwheel switches allow pulse-width selection from 0.1 to 999.9 seconds, or 0.1 to 999.9 milliseconds, depending on the range selected. To indicate how the circuit functions, a general description of a typical one-shot application is used.

The user determines the required one-shot pulse width, for example 800.7 seconds. He must also determine desired output pulse polarity, i.e., (OUT or $\overline{\text{OUT}}$). The time is entered in the thumbwheel switch, the range switch is put in "Seconds", the mode select switch is put at "Monostable" and "Reset/Halt" is depressed momentarily.

To start the cycle the "Start" button is depressed. This gates in the 1 MHz clock from the MK 5009 P through the C/MOS-to-TTL buffer. The first clock pulse is used to strobe the MSD into the variable modulo counter (74192). (Actually the nine's complement is supplied to the counter through the BCD switch multiplex circuitry.) The ÷N counter divides the 1MHz clock by the integer value of the MSD. The states of flip-flops FFA and FFB determine which digit (or decade range) is being processed.

When the Time Out output from the MK 5009 P completes its time cycle, it advances the state counter, selects the next digit to be processed, and then changes the variable modulo counter to correspond to this new digit. If the next digit happens to be a zero, the flip-flops (FFA and FFB) are toggled at the 1 MHz rate until a non-zero digit is found. In the example given (800.7 seconds) after timing of the 800 seconds is complete, the flip-flops would toggle through the second and third digits to ".7", the first non-zero digit, and count the remaining 7/10 second.

However, the one-shot may also be operated in an "astable" mode which results in a square-wave output with a period equal to twice the dial setting. Once the circuitry is started it will free-run until either the mode is changed or the Reset button is depressed.

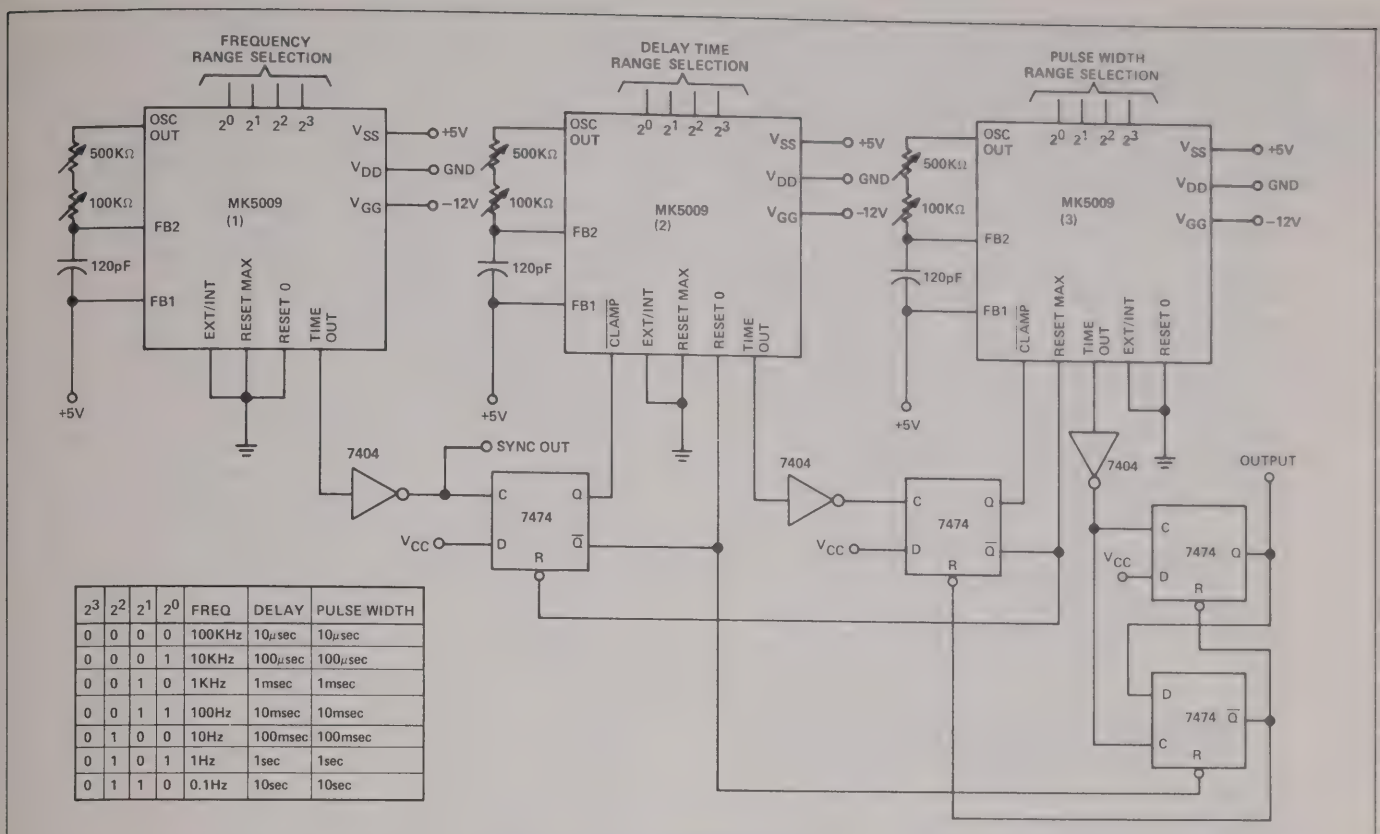
Because of the synchronous nature of the MK 5009 P counters, there should be no timing errors associated with the decade selection switching. The synchronous nature of the MK 5009 P counters and processing the digits from MSD to LSD enables the circuit to operate without being reset and therefore does not introduce an additional time delay.

Further, the potential problem of timing errors at the beginning of a cycle is eliminated, since there is ample time (500 nsec) to load a new digit integer code before the load command is taken away. This is true for either timing range, seconds or milliseconds.

Further Design Applications

This basic design can be extended to accomplish a programmable sequence timer. Any kind of ROM (programmable, fixed mask, or diode matrix) can be used to contain all the times (BCD) codes for the required steps. A state counter of sufficient capacity can be used to control the addressing of the ROM.

Numerous applications for systems of this kind exist wherever a timed sequence of events is required, such as photographic processing, process control, test sequences, and innumerable industrial applications.



2^3	2^2	2^1	2^0	FREQ	DELAY	PULSE WIDTH
0	0	0	0	100KHz	10μsec	10μsec
0	0	0	1	10KHz	100μsec	100μsec
0	0	1	0	1KHz	1msec	1msec
0	0	1	1	100Hz	10msec	10msec
0	1	0	0	10Hz	100msec	100msec
0	1	0	1	1Hz	1sec	1sec
0	1	1	0	0.1Hz	10sec	10sec

FIG. 2: PULSE GENERATOR

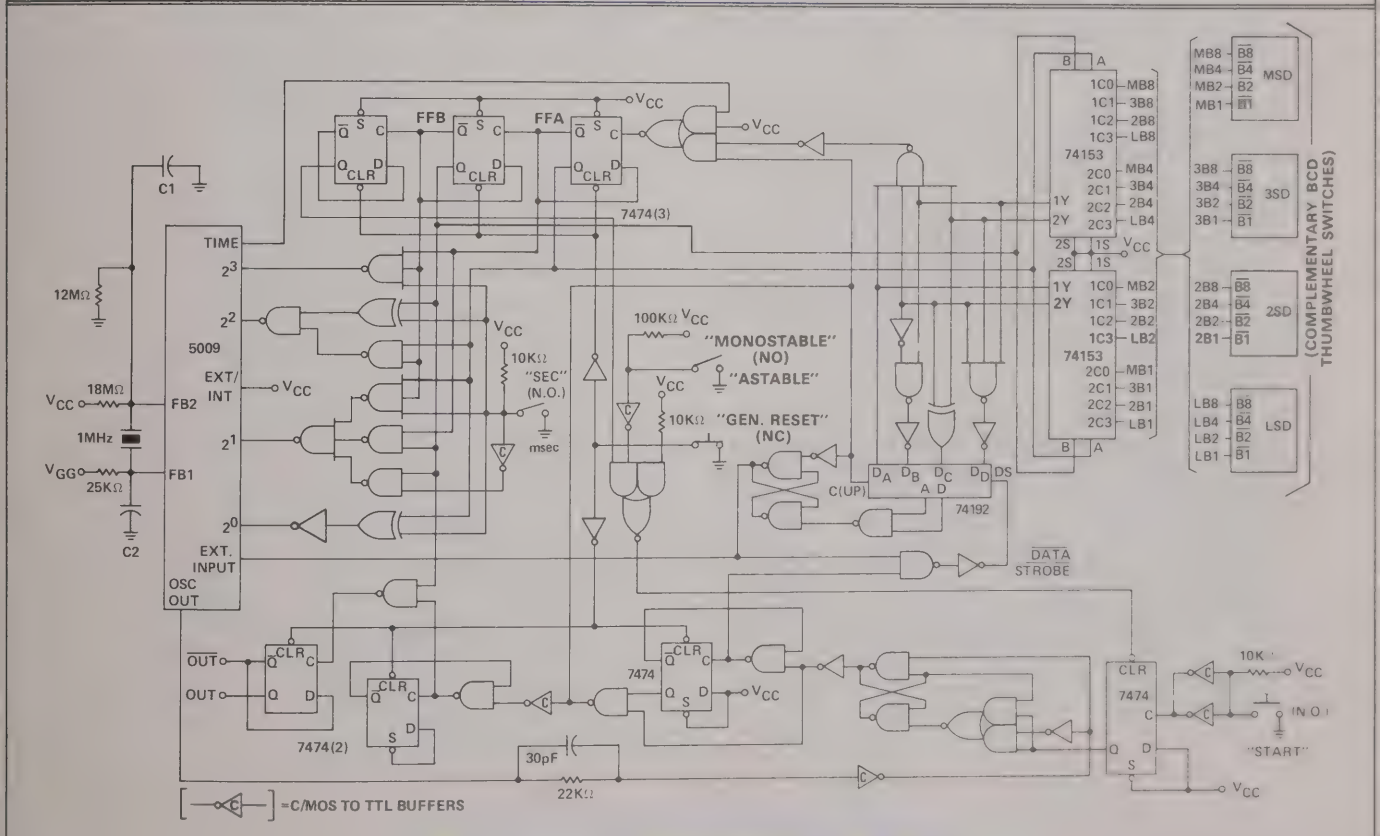


FIG. 3: DIGITALLY-PROGRAMMABLE ONE-SHOT

USE WITH 2.0 MHz CRYSTAL

In some applications a different crystal frequency (such as 2.0 MHz) may be more readily available, although the actual requirements on the output might be decade divisions of 1.0 MHz. Figure 4 shows one way to accomplish this.

A 2.0 MHz crystal is used in the recommended circuit and the frequency at the Oscillator Output pin is divided by 2 by the flip-flop. The 1.0 MHz is then fed back into the chip at the External Input pin. The interface is constructed with C/MOS circuitry since it presents a very high input impedance which does not load down the oscillator output. Use of C/MOS-to-TTL type inverters allows direct drive of the External Input on the 5009 with its internal pull-up resistor.

This circuitry also provides a buffered 1.0 MHz (or 2.0 MHz) signal which can be used as a self-check input for a frequency meter without excessively loading the Oscillator Output.

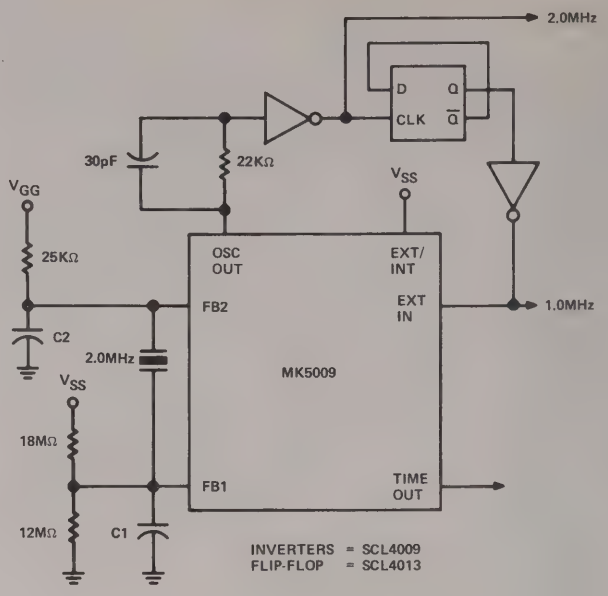


FIG. 4: USE WITH 2.0 MHz CRYSTAL

INTERNAL CONFIGURATION OF THE MK 5009 P OSCILLATOR CIRCUIT

As can be seen in Fig. 5 (a) the basic oscillator section of the MK 5009 P is fairly simple. It consists of two parts: an active device, Q1, for gain in the crystal mode of operation; and a Schmitt trigger and inverting buffer for wave-shaping the waveform at Feedback 2.

In the RC oscillator mode, Fig. 5 (b), Feedback 1 is tied to V_{SS}. This keeps Q1 off and effectively removes it from the circuit. One end of the timing capacitor and one end of the timing resistor are tied to Feedback 2. Osc. Out is connected to the other end of the resistor. The input at Feedback 2 is "squared-up", inverted, and used to drive Osc. Out which causes the RC voltage waveform to change polarity. The nominal upper and lower trip points for the Schmitt trigger are −1.5V and −7.0V respectively.

In the crystal oscillator mode, Fig. 5 (c), Q1 is used as the active device. A resistor, nominally 25KΩ, is placed from Feedback 2 to V_{GG}, serving as the load element for Q1. In practice the resistor should not have a value lower than 15KΩ. The RC product of this load resistor and the crystal loading capacitance should be smaller than $1/f_{XTAL}$, or the RC combination will affect the oscillator frequency. An inductance, or other external load network, can also be substituted for the load resistor. The device, Q1, has a width/length ratio of about 20 and a nominal g_m of 60 μmhos.

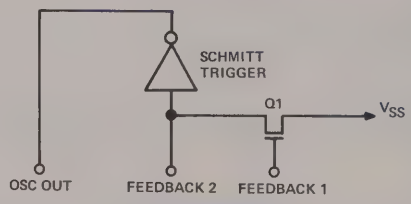


FIG. 5(a)

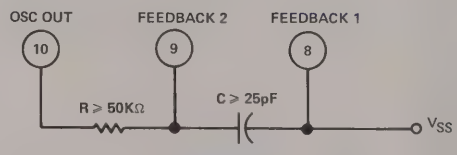


FIG. 5(b)

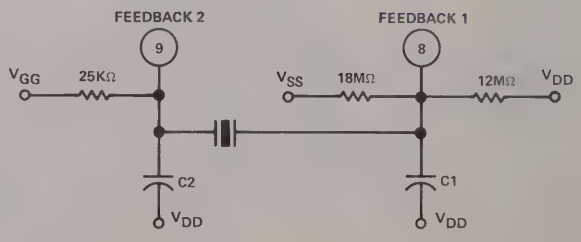


FIG. 5(c)

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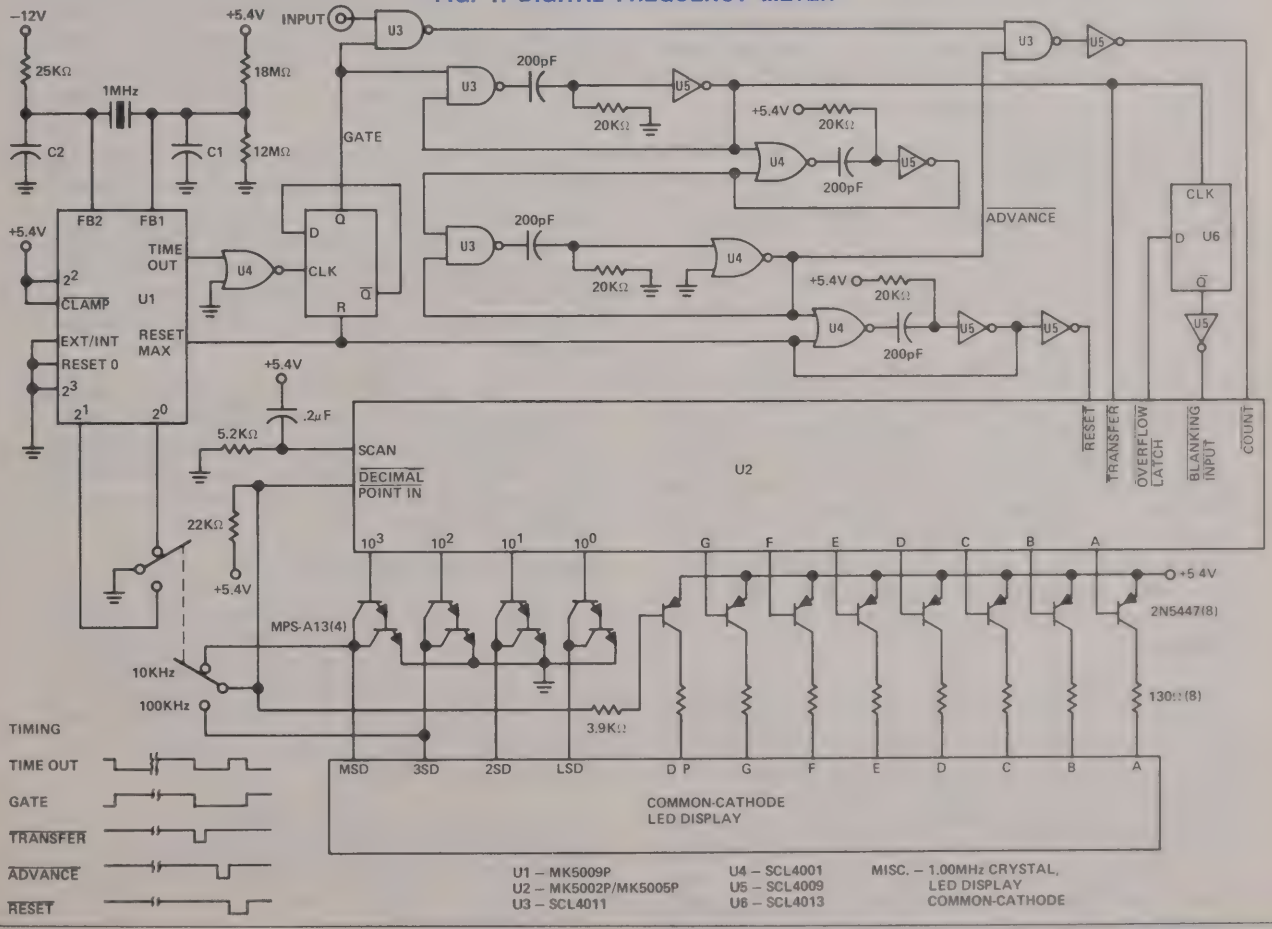


U1 – MK5009P
U2 – MK5002P/MK5005P
U3 – SCL4011
U4 – SCL4001
U5 – SCL4009
U6 – SCL4013
MISC. – 1.00MHz CRYSTAL, LED DISPLAY COMMON-CATHODE

1215 W. Crosby Road, Carrollton, Texas 75006

PULSE GENERATOR

An extremely versatile pulse generator requiring few components is easily built using the MK 5009 P. Three MK 5009 P circuits are used, as shown in Fig. 2, to provide the three essential pulse generator elements: (1) a frequency source to determine pulse repetition rate; (2) a variable time delay; and (3) a pulse width generator.

This circuit provides repetition rates from 0.1 Hz to 100 kHz with delay times and pulse widths from 10μs to 10 seconds. Range selection is obtained by selecting the appropriate divider, so that only three RC circuits are required. This eliminates the requirement for a different RC combination for each decade, commonly found in commercial instruments. Decade selection is accomplished by a binary code at the inputs to each MK 5009 P, which could be provided by a coded rotary or thumbwheel switch. The vernier control is a 500K potentiometer. A 100K potentiometer is used as a trimmer for initial calibration.

External TTL control logic is used to capture the accurately controlled negative edges as they emerge from each MK 5009 P. The Reset and Clamp Inputs allow synchronization and first-cycle accuracy from the time-base circuits.

Other features can be added to the basic circuitry shown in Fig. 2. For example, the output amplitude can be made adjustable by using high-voltage, open-collector TTL circuitry with potentiometer control for amplitude. An extra position can be used on the frequency selection switch for an external trigger source. This trigger source should be connected to the first control D-type latch in lieu of the output from the 5009 (1). The frequency range may even be extended to 1.0 MHz with time delays reduced to 1μs, although some loss in RC stability would occur since the recommended data sheet frequency had been exceeded.

DIGITALLY-PROGRAMMABLE ONE-SHOT

Using the MK-5009 in the circuit shown in Fig. 3 results in a very accurate one-shot which is digitally programmable. Four decades of thumbwheel switches allow pulse-width selection from 0.1 to 999.9 seconds, or 0.1 to 999.9 milliseconds, depending on the range selected. To indicate how the circuit functions, a general description of a typical one-shot application is used.

The user determines the required one-shot pulse width, for example 800.7 seconds. He must also determine desired output pulse polarity, i.e., (OUT or $\overline{\text{OUT}}$). The time is entered in the thumbwheel switch, the range switch is put in "Seconds", the mode select switch is put at "Monostable" and "Reset/Halt" is depressed momentarily.

To start the cycle the "Start" button is depressed. This gates in the 1 MHz clock from the MK 5009 P through the C/MOS-to-TTL buffer. The first clock pulse is used to strobe the MSD into the variable modulo counter (74192). (Actually the nine's complement is supplied to the counter through the BCD switch multiplex circuitry.) The ÷N counter divides the 1MHz clock by the integer value of the MSD. The states of flip-flops FFA and FFB determine which digit (or decade range) is being processed.

When the Time Out output from the MK 5009 P completes its time cycle, it advances the state counter, selects the next digit to be processed, and then changes the variable modulo counter to correspond to this new digit. If the next digit happens to be a zero, the flip-flops (FFA and FFB) are toggled at the 1 MHz rate until a non-zero digit is found. In the example given (800.7 seconds) after timing of the 800 seconds is complete, the flip-flops would toggle through the second and third digits to ".7", the first non-zero digit, and count the remaining 7/10 second.

However, the one-shot may also be operated in an "astable" mode which results in a square-wave output with a period equal to twice the dial setting. Once the circuitry is started it will free-run until either the mode is changed or the Reset button is depressed.

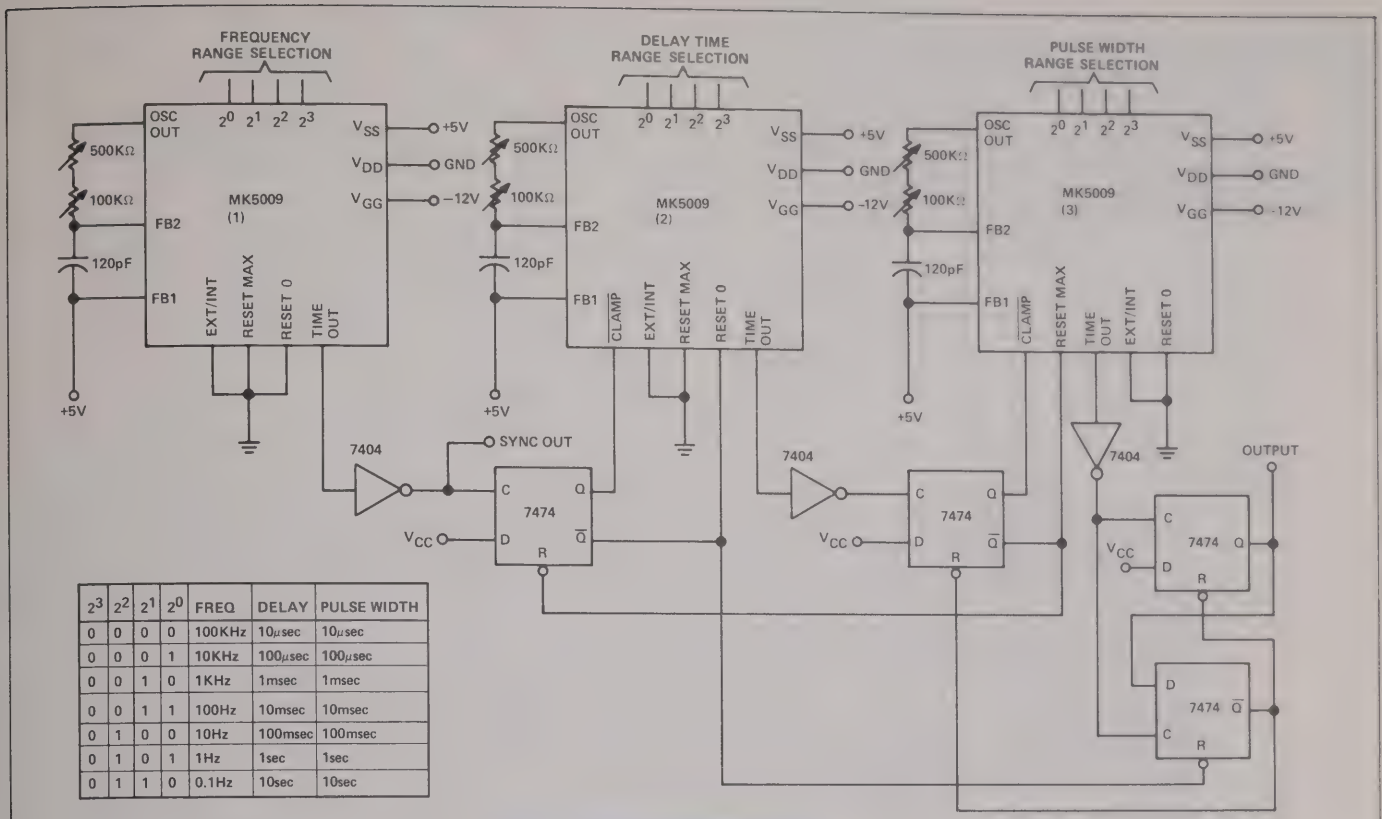
Because of the synchronous nature of the MK 5009 P counters, there should be no timing errors associated with the decade selection switching. The synchronous nature of the MK 5009 P counters and processing the digits from MSD to LSD enables the circuit to operate without being reset and therefore does not introduce an additional time delay.

Further, the potential problem of timing errors at the beginning of a cycle is eliminated, since there is ample time (500 nsec) to load a new digit integer code before the load command is taken away. This is true for either timing range, seconds or milliseconds.

Further Design Applications

This basic design can be extended to accomplish a programmable sequence timer. Any kind of ROM (programmable, fixed mask, or diode matrix) can be used to contain all the times (BCD) codes for the required steps. A state counter of sufficient capacity can be used to control the addressing of the ROM.

Numerous applications for systems of this kind exist wherever a timed sequence of events is required, such as photographic processing, process control, test sequences, and innumerable industrial applications.



2^3	2^2	2^1	2^0	FREQ	DELAY	PULSE WIDTH
0	0	0	0	100KHz	10μsec	10μsec
0	0	0	1	10KHz	100μsec	100μsec
0	0	1	0	1KHz	1msec	1msec
0	0	1	1	100Hz	10msec	10msec
0	1	0	0	10Hz	100msec	100msec
0	1	0	1	1Hz	1sec	1sec
0	1	1	0	0.1Hz	10sec	10sec

FIG. 2: PULSE GENERATOR

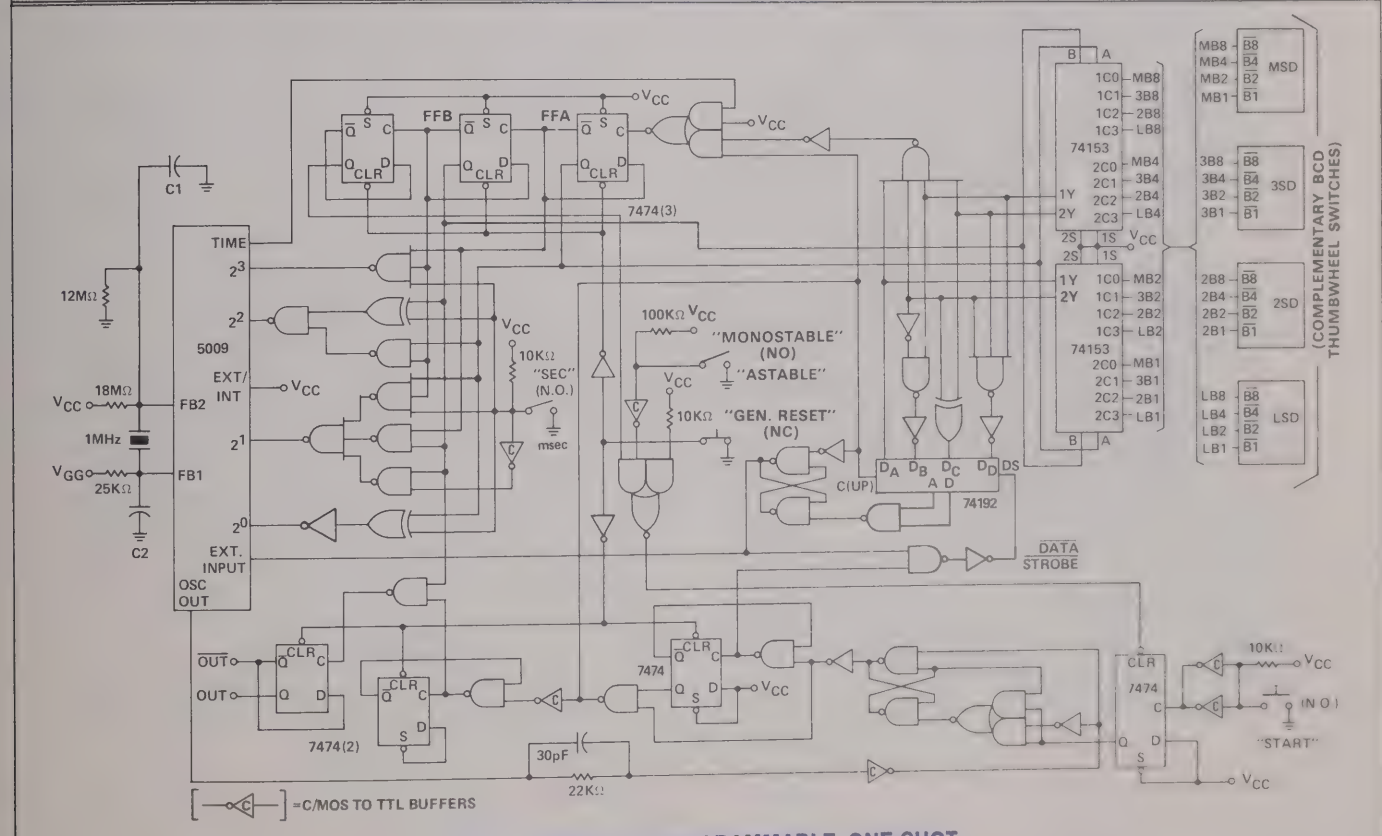


FIG. 3: DIGITALLY-PROGRAMMABLE ONE-SHOT

USE WITH 2.0 MHz CRYSTAL

In some applications a different crystal frequency (such as 2.0 MHz) may be more readily available, although the actual requirements on the output might be decade divisions of 1.0 MHz. Figure 4 shows one way to accomplish this.

A 2.0 MHz crystal is used in the recommended circuit and the frequency at the Oscillator Output pin is divided by 2 by the flip-flop. The 1.0 MHz is then fed back into the chip at the External Input pin. The interface is constructed with C/MOS circuitry since it presents a very high input impedance which does not load down the oscillator output. Use of C/MOS-to-TTL type inverters allows direct drive of the External Input on the 5009 with its internal pull-up resistor.

This circuitry also provides a buffered 1.0 MHz (or 2.0 MHz) signal which can be used as a self-check input for a frequency meter without excessively loading the Oscillator Output.

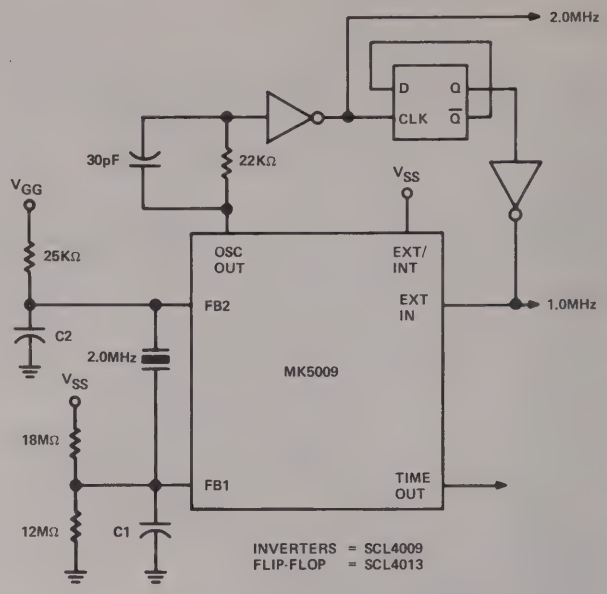


FIG. 4: USE WITH 2.0 MHz CRYSTAL

INTERNAL CONFIGURATION OF THE MK 5009 P OSCILLATOR CIRCUIT

As can be seen in Fig. 5 (a) the basic oscillator section of the MK 5009 P is fairly simple. It consists of two parts: an active device, Q1, for gain in the crystal mode of operation; and a Schmitt trigger and inverting buffer for wave-shaping the waveform at Feedback 2.

In the RC oscillator mode, Fig. 5 (b), Feedback 1 is tied to V_{SS}. This keeps Q1 off and effectively removes it from the circuit. One end of the timing capacitor and one end of the timing resistor are tied to Feedback 2. Osc. Out is connected to the other end of the resistor. The input at Feedback 2 is "squared-up", inverted, and used to drive Osc. Out which causes the RC voltage waveform to change polarity. The nominal upper and lower trip points for the Schmitt trigger are −1.5V and −7.0V respectively.

In the crystal oscillator mode, Fig. 5 (c), Q1 is used as the active device. A resistor, nominally 25KΩ, is placed from Feedback 2 to V_{GG}, serving as the load element for Q1. In practice the resistor should not have a value lower than 15KΩ. The RC product of this load resistor and the crystal loading capacitance should be smaller than $1/f_{XTAL}$, or the RC combination will affect the oscillator frequency. An inductance, or other external load network, can also be substituted for the load resistor. The device, Q1, has a width/length ratio of about 20 and a nominal g_m of 60 μmhos.

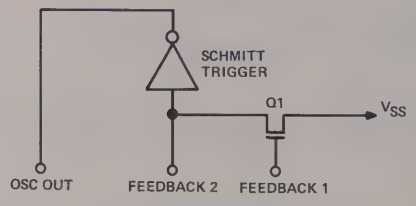


FIG. 5(a)

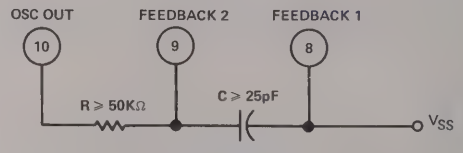


FIG. 5(b)

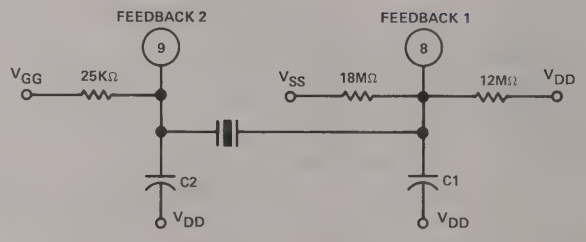


FIG. 5(c)

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MOSTEK

MOS CIRCUIT DEVELOPMENT FOR THE HP-35

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APPLICATIONS NOTE

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MOS CIRCUIT DEVELOPMENT FOR THE HP-35

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Hewlett-Packard
Palo Alto, California

Robert J. Paluck
Mostek Corporation
Carrollton, Texas

Background

HEWLETT-PACKARD: Shortly after the HP 9100A calculator, was announced in March 1968, William Hewlett expressed a desire that the next design be one-tenth the volume and one-tenth the cost. After a trip to Japan in the summer of 1970 and a look at some of the portable four-function calculators being developed he reiterated his previous wish for a pocket size scientific calculator.

The challenge was presented to the corporate laboratories, where the original designers of the 9100 still resided. Work on an architecture was begun in October 1970 and a presentation on the feasibility made to management in February 1971. Although there were pressures to orient the calculator toward the large volume general business user, the final decision was to stick to the scientific market better understood by HP.

It was decided very early to have the custom MOS design done outside HP. Although we had some MOS experience internally, the high density, low power dynamic circuit design required had never been attempted. The company is often eager to take on challenges in technology, but the importance of a rapid, low risk development precluded an in-house source.

MOS Requirements

The MOS requirements were quite difficult. To achieve the required functional density we went to a totally serial design, which reduced interconnections both internal to the chip and between chips. However, the complex algorithms to compute transcendental functions require many multiplications, forcing a relatively high clock rate. We felt a 200 KHz bit rate could achieve the goal of a one second maximum computation time for any function.

On top of the requirements for high density and high speed was the need for low power. The size and volume specification was set by Hewlett's shirt pocket; this meant few and small batteries. Four hours was set as the goal for calculator operating time.

In March 1971 we sent a request for quotations for a three chip system to seven vendors. At first a two chip partitioning was proposed but preliminary talks with vendors indicated at least three chips would be required. The request included complete logic drawings of the three circuits and some rough electrical specifications. Figure 1 shows a block diagram of the system.

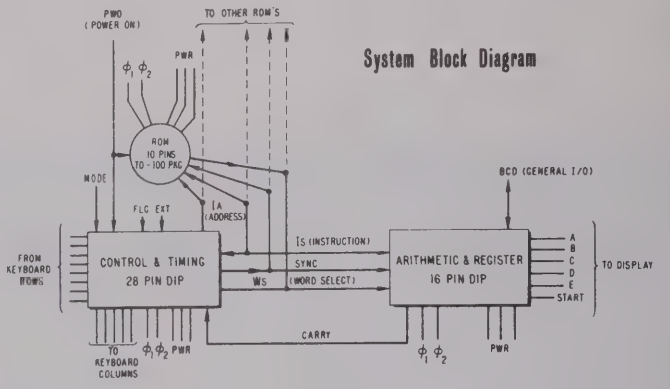

FIGURE 1

MOS Proposal

MOSTEK: We received Hewlett-Packard's RFQ just after our announcement of having produced the first four function calculator on a chip. The request specified that the three chips were to be used in a "battery powered portable instrument". Although we could guess from the logic diagram that the system had processor capabilities, we did not know what the final product was to be.

The three circuit types were the Instruction ROM, the Arithmetic and Register Chip, and the Timing and Control Chip. Table 1 is provided as an indication of the logic complexity and packaging requirement for each circuit. The electrical requirements stated that the system of chips be low powered and operate at 200 KHz. Although we could forsee individual problems in each circuit type, the major challenge would be in designing these complex chips to be low powered, and with chip sizes small enough to fit into the required packages.

CIRCUIT TYPE	LOGIC GATES	FLIP-FLOPS	ROM STORAGE	PACKAGE	FINAL CHIP SIZE (in milli-inches)	NOMINAL POWER (in milli-watts)
Instruction ROM	100	30	256 X 10	10 Pin TO-5	126 X 134	3
Arithmetic and Register	335	460	-	16 Pin C-DIP	156 X 200	20
Timing and Control	340	55	25 X 58	28 Pin C-DIP	150 X 212	50

TABLE 1

Gearing Up For Production

HEWLETT-PACKARD: The speed with which the HP-35 was developed, approximately one year from concept to production, was bound to create some problems. The usual production learning problems affected all parts, including the MOS vendors. Primarily, however, we failed to plan for the hugh success the HP-35 has achieved. Orders have been three times the expected level, forcing a calculator delivery time which at one time was 12 weeks. Once the real demand for the HP-35 was realized it still took about 3-6 months to adequately increase the production.

Present Production

HEWLETT-PACKARD: Production is now running very smoothly, keeping up with the order rate. This high volume, low-cost instrument is a new business for HP, and necessity has made us learn very rapidly. In terms of customer response, the HP-35 is the most successful HP product ever introduced. The price is 1/10 that of the 9100, with 1/80 the volume. We are grateful to our MOS suppliers for the high quality, reasonably priced components which make it possible.

REFERENCES:

1. The "Powerful Pocketful": An Electronic Calculator Challenges the Slide Rule, by Thomas M. Whitney, France Rodé, and Chung C. Tung. Hewlett-Packard Journal, June, 1972.

2. Implanted Depletion Loads Boost MOS Array Performance, by Bob Crawford. Electronics, Vol. 45, No. 9, pp. 85-90, April 24, 1972.

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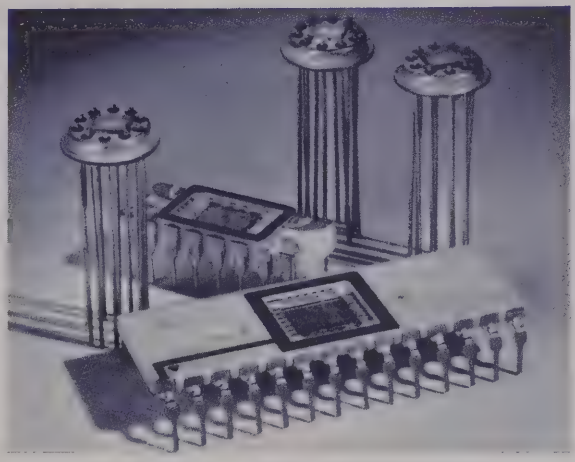
POCKET COMPUTATION
from Hewlett Packard

WE'RE ON THE INSIDE!

The HP-35 pocket calculator is available *today*. A super slide rule, this electronic wonder challenges a computer in its problem-solving capability. People have talked about it for years, but HP made it work . . . a breakthrough product offering an unprecedented combination of size, multifunction capability, accuracy and speed. How is it practical? Through creative, MOS/LSI design, using ion-implanted, depletion-mode technology. A technology pioneered, proven and volume-manufactured by MOSTEK.



MOSTEK MOS circuits custom designed for Hewlett Packard.

What kind of performance does implanted MOS/LSI provide? Here's a summary of the micro-processor developed for the HP-35:

Low Power: 90 mw (typical) for the sum of all five complex MOS arrays

Very Complex Chips: The arithmetic chip alone contains 3600 transistors

Immunity to Battery Voltage Variation: Specifications called for ±16.6%. This was exceeded with the micro-program storage chip operating from 3.5 to 30 V, typically.

Multi-Source Production Capability: MOSTEK pioneered the process; other sources are now following our lead.

MOSTEK's design team made implanted MOS work for Hewlett Packard. Can we do the same for you? For more information, call Marketing Assistance at (214) 242-0444, or contact your nearest MOSTEK sales office listed below.

NOTE: The circuits utilized for the HP-35 are proprietary to Hewlett Packard and not available for general sale. For information on the pocket calculator, write: Advanced Products, Hewlett Packard, 10900 Wolfe Road, Cupertino, Calif. 95014.

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AN-106-FEB. 73

MOS
CLOCK CIRCUIT
MK 5017 P

APPLICATIONS NOTE

BY LARRY SULLIVAN, MOSTEK CORPORATION

SEE HOW IT WORKS
Digital Clock On A Chip

Twelve- or 24-hour displays, alarm, snooze-alarm and clock-radio formats are offered in three MOS LSI circuits.

by LARRY SULLIVAN*

A NEW FAMILY OF THREE MOS IC'S FOR use in electronic digital clocks makes possible several different types of "single chip" clocks. These devices have been introduced by Mostek Corporation of Carrollton, Texas.

All members of this "clock family" are six-digit clocks that display time in hours, minutes, and seconds. If only an hours and minutes clock is desired the same IC may be used with only the two hours and two minutes digits connected to the display. Outputs from these clocks may be connected directly to fluorescent-anode display tubes. The high-voltage output transistors allow fluorescent-anode display tubes to be driven directly.

The MK 5017 P clock circuits are available now in an alarm clock version, the MK 5017 P AA; a clock radio clock, the MK 5017 P AN; and a unique combination clock/calendar the MK 5017 P BB. Time may be displayed in either 12-hour or 24-hour formats.

The standard United States 60-Hz power line frequency may be used as a reference. If the clock is intended for overseas operation where 50 Hz is the standard power line frequency, the 50-Hz input frequency reference may be selected. The MK 5017 P clock senses the power supply voltage and, if loss of power is detected, displays all "eights". A backup battery may be used as a power supply during temporary power loss. An adjustable 50-Hz or 60-Hz oscillator is included on the chip to furnish the frequency reference during temporary loss of power.

The clock circuits require only a single power-supply voltage, simplifying power supply design.

Time setting is easy, a matter of depressing and holding push-buttons which allow the internal counters to increment at a 2-Hz rate. Each of the minutes digits and the hours digits may be set individually with no "carrys" generated to the more significant digits. Thus, there is no "overrun" when setting the counter to a time such as 2:59. In a counter in which "carrys" are allowed between digits it is very easy to increment the minutes "9" by one extra count and change all three digits so that the time reads 3:00. This makes it necessary to reset the hours, tens of minutes, and minutes all over again.

How it works

Figure 1 is a functional block diagram of the MK 5017 P digital clock circuit. A 1-Hz reference frequency is generated for the time counter by the shaper-divider network from either a 50-Hz or a 60-Hz input. The 50/60-Hz input frequency may be derived from the ac line or can be provided by an external crystal-controlled oscillator and frequency divider for portable or automobile applications. When the ac

*Mostek Corp., 1215 West Crosby Road, Carrollton, Tex.

rate. If both the hours and the minutes switches are closed simultaneously the "tens-of-minutes" digit advances twice each second.

Enabling the alarm is accomplished by closing the switch located at the intersection of the *D4* and KB lines. When coincidence is detected between the time counter and the alarm counter, the alarm tone is generated for one hour if the enable alarm switch is closed.

When the alarm "goes off" the snooze switch located at the intersection of the *D4* and KA lines may be momentarily depressed to inhibit the alarm. After seven minutes the alarm will go off again. This cycle may be repeated indefinitely.

Twelve or twenty-four hour time displays may be selected at any time without disturbing the time counter. Closing the switch located at the intersection of the *D3* and KA line results in a twenty-four hour display.

For operation from a 50-Hz reference frequency, the switch located at the intersection of the *D3* and KB lines may be closed. When this switch is open, the clock assumes a 60-Hz reference frequency.

MK 5017 P AN

Clock radio clocks may be built using the MK 5017 P AN. This circuit includes all of the features normally found on a clock radio clock. Both the alarm clock – MK 5017 P AA, and the clock-radio clock – MK 5917 P AN are shown in Fig. 2. The circuitry shown by dashed lines applies to the clock-radio clock. The remaining circuitry is common to both.

In addition to all of the features found on the alarm clock circuit the clock-radio circuit also has a radio sleep output that may be used to keep a radio or other appliance on for selected periods of time up to a maximum of two hours.

Radio sleep operation is selected by closing switch SL at the intersection of the *D1* and KA lines in the input matrix. The switches located at the intersection of the *D1* and KB lines (SL1) at the intersection of the *D2* and KB lines (SL2), and at the intersection of the *D2* and KA lines (SL2), are used to select the desired sleep time. There are eight possible combinations that may be achieved with these three switches, so a total of eight different sleep times may be selected. The switches are arranged in a binary code with the switch designated as SL1 being the least significant bit. The switch designated as SL4 is the most significant bit. The times that may be selected, along with the switch closures required to program these times, are presented in table.

SLEEP SWITCH TABLE

Radio Sleep Time	*Switch Combinations*		
	SL4	*SL2*	*SL1*
10 Min	open	open	open
20 Min	open	open	closed
30 Min	open	closed	open
40 Min	open	closed	closed
50 Min	closed	open	open
60 Min	closed	open	closed
90 Min	closed	closed	open
120 Min	closed	closed	closed

After selecting the desired radio sleep time from the table, close the sleep switch to start the timing interval. It is not necessary to install three switches and remember the binary code for sleep times. Instead, an eight-position three-pole rotary switch may be used to easily and rapidly select sleep times.

In addition to the radio sleep feature the MK 5017 AA also has a radio WAKE/SLEEP output. The radio WAKE/SLEEP output is operative during RADIO WAKE and RADIO SLEEP operation. For RADIO WAKE operation the radio WAKE/SLEEP output is on when the alarm counter and the time counter become equal. The radio WAKE/SLEEP output remains active for one hour during *radio wake* operation.

A display inhibit pin is included on the clock-radio clock circuit. All of the segment- and digit-output transistors are disabled (turned off) when the inhibit pin is connected to V_{SS}. This feature makes it possible to build a multifunction clock using only one display, without any external multiplexing circuits. **R-E**

MK 5017 P BB

A combination clock/calendar display may be built using the MK 5017 P BB combination clock/calendar circuit. The MK 5017 P BB clock/calendar has almost the same functional pins as the MK 5017 P AA alarm clock circuit with two exceptions. The AM, 1 HZ, and TONE pins have been replaced by the INHIBIT pin and an ALT pin. All of the digit and segment output transistors are disabled when the INHIBIT pin is connected to V_{SS}. This provides a convenient means of disabling the display outputs without interfering with the timekeeping of the circuit. This makes it possible to build such multiple function devices as combination clock calculators. The ALT output is at a logical one, near V_{SS}, to indicate that time is being displayed. The ALT output switches to a logical zero, near V_{DD}, while calender information is being displayed. The MK 5017 P BB input matrix is similar to that for the MK 5017 P AA and the MK 5017 P AN circuits. A time set switch is located at the intersection of the D6 digit line and the KA multiplexed input line. The alarm set switch located at the intersection of the D6 digit line and the KB multiplexed input line has been replaced by a calendar set switch. With the calendar set switch closed, the hours and minutes pushbutton switches may be used to set the calendar. The hours pushbutton switch may be used to set months on the calendar display and the minutes pushbutton switch may be used to set days. An ACS switch is located at the intersection of D4 digit line and the KA input line. This switch may be used to force the ALT output to a logical zero. When the ATS switch at the intersection of D4 digit line and the KB input line is closed, it forces the ALT output to a logical one and selects a time only display. Operation of the 12 or 24 hour display select switch located at the intersection of the D3 and KA lines, and the 50/60 Hz select switch located at the intersection of the D3 digit line and the KB input line, is the same as described for the alarm clock and the clock radio clock circuit. The clock is in the RUN mode when both the time set switch and the calendar set switch are open. In the RUN mode the display alternates between the time display and calendar display displaying time for 8 seconds and calendar information for 2 seconds. The calendar is a 31 day calendar and must be reset at the end of each month that does not have 31 days. Calendar information is presented as a numerical representation of the month and day of the month.

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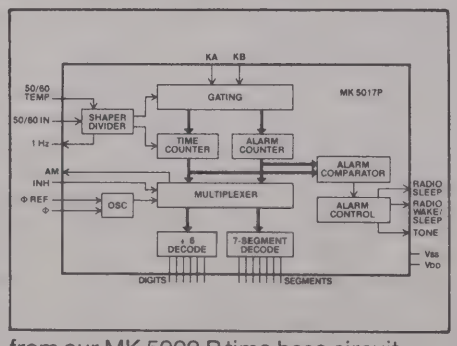
MOSTEK's new digital clock circuit...

A CLOCK FOR ALL REASONS

Designing clock systems? Say, alarm clocks? Clock radios? Calculator clocks? Calendar clocks? Stop watches? Industrial timers?

Then meet our MK 5017 P digital clock circuit. It's microprogrammable so we can tailor it to your exact application. Three standard versions are already available: the MK 5017—AA alarm clock; MK 5017—AN alarm clock/clock radio; and MK 5017—BB calendar clock. Look at these key features:

- 4 or 6-digit 7-segment display plus AM/PM indication (all versions)
- Clock radio features including sleep delay (AN)
- 12 or 24-hour operation and display (all versions)
- Snooze feature (AA, AN)
- Quick, convenient time and alarm setting (all versions)
- 50 or 60 Hz input—standard line or



from our MK 5009 P time base circuit (all versions)

- Alarm tone generated on-chip; no external oscillator required (all versions)

Interfacing with your display is easy. If you're using luminescent anode tubes, our 5017 will drive your display *directly* (no driver transistors necessary). Or, you can interface with LED, incandescent, gas discharge tube or light emitting film displays with minimal additional circuitry. And if you're using some other type, check our latest applications literature to shed some light on your problem.

It's easy to make time work for you. Just contact your nearest MOSTEK sales office, distributor or representative... today!

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Miscellaneous

MOSTEK CORPORATION

ALTERNATE SOURCE DIRECTORY

MOSTEK Part No.	Organization/Description	TTL/DTL Compatible	Max Clock Max Access	Package	Pin-for-Pin Alternate
MK 1002 L MK 1002 P	2 X 128-bit Shift Register (static)	yes	1 MHz	TO-100 16 pin CDIP	(TI) TMS3114JC
MK 1007 P	4 X 80-bit Shift Register (dynamic)	yes	2.5 MHz	16 pin CDIP	(TI) TMS 3409JC
MK 2000 P MK 2002 P	ROM, 64 X 5 X 7-bits (column out), MK 2002 P is an ASCII encoded character generator		700ns	28 pin CDIP	(TI) TMS 4100 TMS 4103 JC
MK 2300 P MK 2302 P	ROM, 64 X 5 X 7-bits (column out), MK 2302 P is an ASCII encoded character generator	yes	1μs	24 pin CDIP	(Fchld) 3257
MK 2400 P MK 2408 P	ROM, 256 X 10-bits (static) ASCII encoded character generator (row out)	yes	550ns	24/28 pin CDIP	(AMI) MA51M (TI) TMS 2300
MK 2500 P MK 2503 P	ROM, 512 X 8 or 1024 X 4 (static) ASCII-to-EBCDIC, EBCDIC-to-ASCII code converter	yes	1μs	24 pin CDIP	(National) MM5232
MK 2600 P MK 2601 P	ROM, 512 X 8 ASCII-to-EBCDIC, EBCDIC-to-ASCII code converter	yes	700ns	24 pin CDIP	(Fchld) 3514
MK 4006 P	RAM, 1024 X 1-bit (dynamic-refresh at 2ms rate-min)	yes	400ns	16 pin CDIP	(AMI) S4006
MK 4007 P	RAM, 256 X 1-bit (static)	yes	.9μs	16 pin CDIP	(Intel) 1101, 1101 (Sig) 2501 (Intersil) IM7501C (TI) TMS 1101JC
MK 4008 P	RAM, 1024 X 1-bit (dynamic refresh at 2ms rate-min)	yes	500ns	16 pin CDIP	(AMI) S4006

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